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Low-Loss Amorphous Silicon Multilayer Waveguides Vertically Stacked on Silicon-on-Insulator Substrate

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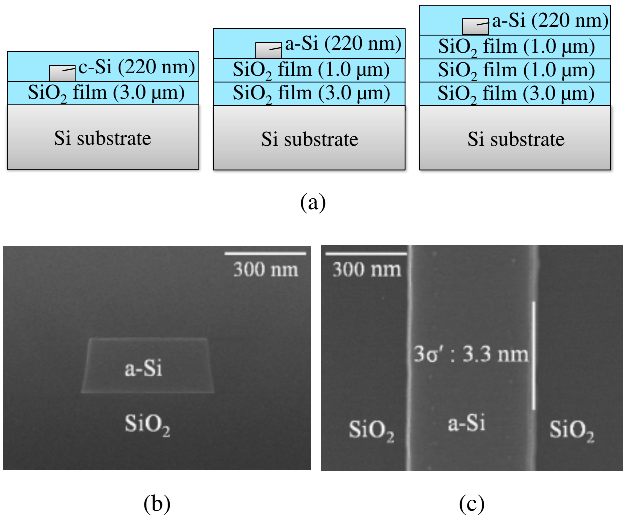
Low-loss amorphous-silicon (a-Si) waveguides comprising three vertically stacked layers prepared on silicon-on-insulator substrates are demonstrated. We have fabricated multilayer a-Si waveguides and investigated their loss characteristics; this is the first such investigation to our knowledge. All the process temperatures were regulated below 400 °C for the complementary metal oxide semiconductor (CMOS) backend process compatibility. When the surface roughness and sidewall roughness were decreased, the propagation loss decreased to 3.7 dB/cm even in the case of the third layer a-Si waveguide. Such low-loss waveguides can be effectively applied to realize multilayer stacked optical devices.

Optical interconnections on silicon (Si) large-scale integrated circuits (LSIs) are attracting attention as a breakthrough technology for overcoming the performance limitations of electrical interconnections as well as for realizing high-density systems-on-chip (SoCs).[1,2] Further, it is expected that the basic material for these optical interconnections will be Si-based materials since they can be integrated with Si-LSI, thereby ensuring sufficient process compatibility. In addition, Si has a large refractive index difference when paired with SiO_2 and enables the fabrication of sub-micron optical waveguides, thereby leading to high-density optical circuits. Several parts of optical components having silicon-on-insulator (SOI) substrates have already been demonstrated.[3–5]

However, in order to integrate the optical components on an LSI through backend processes, all the fabrication processes for the optical components should be regulated to below 400 °C in order to avoid damages to the complementary metal–oxide–semiconductor (CMOS) layer. Amorphous silicon (a-Si) is the most promising material for optical circuits since it can be deposited under low-temperature conditions by plasma-enhanced chemical-vapor-deposition (PECVD).[6] In addition, multilayer stacking can be realized by depositing a-Si and SiO_2 alternately, and high-density three-dimensional optical circuits can thereby be realized on the LSI. Recently, the ultrafast nonlinear characteristics of a-Si waveguides have attracted additional attention.[7] Many researchers have demonstrated low-loss a-Si waveguides, while a few researches have been conducted on light transmissions between a-Si waveguides placed on top and crystalline Si (c-Si) waveguides placed at the bottom.[8–11] However, to our knowledge, there have been no reports on the characteristics when more than three stacked layers of Si waveguides are placed. In this paper, we have investigated, for the first time to our knowledge, the loss characteristics of a-Si waveguides prepared through multilayer stacking processes and the dependence of the performance on the fabrication processes.

Multilayer a-Si waveguides were fabricated on a SOI wafer consisting of a 3-µm buried oxide (BOX) layer and a 220-nm c-Si layer. The core width and height of the a-Si waveguides were 450 and 220 nm, respectively, for all the layers. The schematic images of each layer are illustrated in Fig. 1(a), and the cross-sectional scanning electron microscope (SEM) image of the third layer waveguide is shown in Fig. 1(b). The fabrication process is described below.



(a)

(b) (c)

Fig. 1. (Color online) (a) Schematic diagrams of c-Si (first layer) and a-Si waveguides (second and third layers) and (b) cross-sectional and (c) top SEM images of the third layer of the a-Si waveguide formed by PP-RIE.

The waveguides were patterned by electron beam lithography (EBL) with a double-layered positive resist Zeon ZEP520A and with a C_{60}-containing microcomposite in order to enhance the etching selectivity between the resist and Si-films.[12] The waveguide pattern was formed by dry etching wherein two types of dry etching systems—parallel-plate reactive-ion-etching (PP-RIE) and inductively-coupled-plasma (ICP) RIE—were used. For the second layer fabrication, c-Si layer was removed and 1-µm-thick SiO_2 was deposited by PECVD from tetraethyl orthosilicate (TEOS) [TEOS flow rate: 14 sccm, O_2 flow rate: 300 sccm, gas pressure: 120 Pa, power: 250 W, deposition temperature: 300 °C]. Subsequently, a-Si was deposited by PECVD on the SiO_2 layer as the second layer. The third layer was also fabricated by repeating the previous processes. The SEM image from the top of the third layer waveguide is shown in Fig. 1(c). The sidewall roughness values ($3\sigma'$ values; σ' is the standard deviation) of the waveguides after PP-RIE and ICP-RIE were measured by

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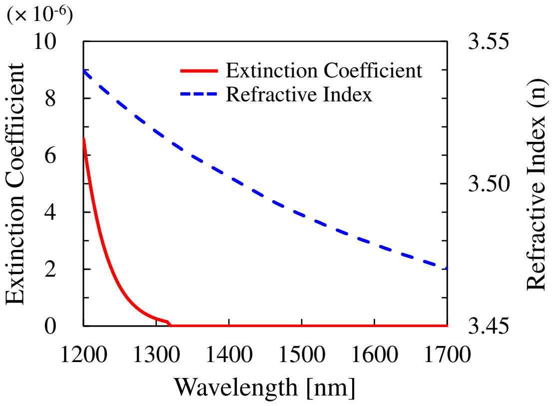

Fig. 2. (Color online) Wavelength dependence of the refractive index and extinction coefficient for a-Si film.

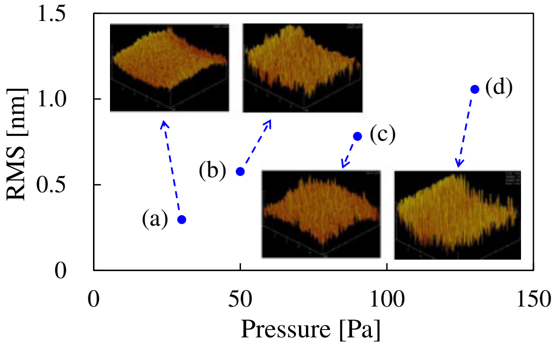

Fig. 3. (Color online) Surface roughness of a-Si film as a function of deposition pressure in the form of AFM images, (a) 30, (b) 50, (c) 90, and (d) 130 Pa.

Table I. Surface roughness of each layer (RMS).

Measured point	First	Second		Third	
	(c-Si)	130 Pa	30 Pa	130 Pa	30 Pa
σ_{Top} (nm)	0.17	1.06	0.30	1.03	0.52
σ_{Bottom} (nm)	0.18	0.24	0.24	0.37	0.36

the function of the SEM (Hitachi S-5000) to be 3.3 and 2.4 nm, respectively; further, the sidewall angles of each waveguide were 81 and 85°, respectively.

It is well known that a-Si tends to have high optical absorptions under certain conditions. We measured the extinction coefficient and refractive index of the deposited a-Si by using the ordinary ellipsometry method. The deposition conditions were as follows. SiH_4 flow rate: 100 sccm, Ar flow rate: 100 sccm, power: 100 W, and deposition temperature: 300 °C. Figure 2 shows the wavelength dependence of the refractive index and extinction coefficient for the a-Si film. From the results, the real part of the refractive index was 3.48, and the material absorption in our deposition film at 1.55-µm wavelength can be expected to be negligible.

The surface roughness of each layer before and after the deposition of the a-Si layer was measured by using an atomic force microscope (AFM); these roughness values are listed in Table I as root-mean-square (RMS) values. σ_{bottom} refers to the surface roughness before a-Si deposition for each layer (in other words, the roughness of the top of the SiO_2 film). For the first layer (c-Si), the value was measured after etching the c-Si film. σ_{top} refers to the roughness values after the a-Si deposition. The table lists the RMS roughness for the a-Si films under the deposition pressures of 30 and 130 Pa during PECVD. The top surface roughness of a-Si film is inferior to that of c-Si film when the deposition pressure was 130 Pa.

The top surface roughness as well as the corresponding AFM image as a function of the deposition pressure is shown in Fig. 3. As the deposition pressure decreased, the surface roughness reduced from 1.06 nm (130 Pa) to 0.30 nm (30 Pa), and this can be attributed to increases in the migration length at lower deposition pressures. When the deposition pressure was 30 Pa, the surface roughness was 40–50% higher after the deposition of the a-Si layer and approximately twice and thrice that of the c-Si layer after the depositions of the second and third a-Si layers, respectively.

The propagation losses of a-Si waveguides fabricated by PP-RIE [CF_4 gas flow: 10 sccm, pressure: 0.3 Pa, bias power: 20 W, waveguide width: 450 nm, sidewall roughness: 3.3 nm ($3\sigma'$ value), sidewall angle: 81°] were measured by coupling transverse-electric (TE) polarized light from a tunable laser emitting at around 1.55-µm wavelength. The light was coupled to the waveguides through tip lensed single-mode fibers, and the propagation losses were calculated by using the cutback method. For the deposition pressure of 130 Pa, the propagation losses of the first c-Si layer, the second, and the third a-Si layers were 6.0, 10.2, and 12.0 dB/cm, respectively. The propagation loss of the second layer a-Si waveguide with the deposition pressure of 30 Pa was 7.0 dB/cm, i.e., only 1 dB/cm higher than that of the first layer c-Si waveguide.

Previous experiments had focused on the surface roughness of multilayer waveguides. In our study, we changed the etching machine from PP-RIE to ICP-RIE in order to cut down the sidewall roughness. Low process pressures can be applied by using ICP-RIE that assists the directionality of the ion flux in the chamber, and moreover, these characteristics lead to better vertical shapes during etching process.[13] We fabricated multilayer a-Si waveguides up to the third layer with ICP-RIE [CF_4 gas flow: 10 sccm, pressure: 0.03 Pa, ICP power: 5 W, bias power: 150 W]. The deposition pressure of 30 Pa was used for a-Si; here were no noticeable changes in the surface roughness between PP-RIE and ICP-RIE. Further, the waveguide width was changed to 500 nm. We assumed that the propagation loss reduces with wider widths even though the effect is negligible. The sidewall angle improved from 81 to 85° when the ICP-RIE etching process was used, and the sidewall roughness ($3\sigma'$ value) was estimated to be 2.4 nm. The propagation losses of the first layer c-Si waveguide and the second and third layer a-Si waveguides were measured to be 1.6, 3.8, and 3.7 dB/cm, respectively.

To determine the reasons for the propagation loss degradation with multilayer waveguides, we plotted the measured propagation losses against the sum of the RMS values of the top and bottom surface roughness values $(\sigma_{\mathrm{top}}^2 + \sigma_{\mathrm{bottom}}^2)^{1/2}$ (Fig. 4). The solid line in the figure shows the calculated results of the scattering loss after considering

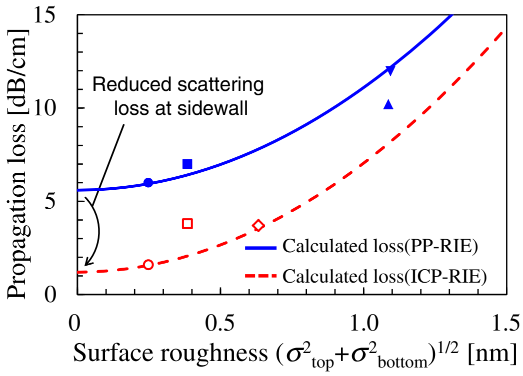

Fig. 4. (Color online) Measured losses (diamonds) and calculated losses due to the surface roughness of the Si waveguides. (Further information about plotted data is listed in Table II.)

the surface roughness and sidewall roughness for the PP-RIE-etched waveguides.[14–16] The scattering loss at the sidewall was assumed to be 5.6 dB/cm. The measured propagation losses agreed well with the calculated ones, and this indicates that the primary cause of the propagation loss difference between the c-Si and a-Si waveguides is the scattering loss from the surface and not the material absorption of a-Si. Therefore, reducing the surface roughness as well as side wall roughness is very important for fabricating low-loss a-Si waveguides.

The relationship between the scattering loss and surface roughness is also calculated as a dashed line in Fig. 4 for the ICP-RIE etched waveguides; the scattering loss at the sidewall was estimated to be 1.2 dB/cm. The propagation loss drastically reduced in these samples as a result of the improvements in the sidewall roughness. All the propagation losses of each waveguide are summarized in Table II.

In summary, we have fabricated multilayer a-Si waveguides and investigated their loss characteristics for the first time to our knowledge. Further, we have confirmed the deterioration of the surface roughness for multilayer waveguides. The surface roughness and sidewall roughness dependence of the propagation loss have been described and the effects of the roughness values have been estimated separately. When the deposition pressure of a-Si was decreased from 130 to 30 Pa, the scattering from the surface roughness decreased, leading to improvements in the propagation loss. The scattering loss from the sidewall roughness also decreased when the etching method was changed from PP-RIE to ICP-RIE. The propagation losses of the first layer c-Si waveguide and second and third layer a-Si waveguides were obtained as 1.6, 3.8, and 3.7 dB/cm, respectively.

Table II. The propagation loss of each layer waveguide.

Etching method	First	Second		Third	
	(c-Si)	130 Pa	30 Pa	130 Pa	30 Pa
PP-RIE (dB/cm)	● 6.0	▲ 10.2	■ 7.0	▼ 12.0	—
ICP-RIE (dB/cm)	○ 1.6	—	□ 3.8	—	◇3.7

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