Crystalline/Amorphous Si Integrated Optical Couplers for 2D/3D Interconnection

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***Abstract*—The in-plane and interlayer waveguide-type couplers between crystalline Si and amorphous-Si:H wire waveguides, for 2D/3D hybrid-material integration are presented in this paper. The in-plane-type coupler achieves stable coupling between two waveguides by using tapers located at the tips of the waveguides. The interlayer-type coupler can connect two waveguides, despite an interlayer distance of 1 μm, with a simple process flow, by introducing a trident structure. An experiment was conducted in which the in-plane and interlayer-type couplers realized low coupling losses (coupling efficiencies) of 0.16 dB (96%) and 0.49 dB (89%) per coupler, respectively.**

***Index Terms*—A-Si:H waveguide, multilayer, nonlinearity, trident.**

I. Introduction

An optical interconnection is regarded as an effective technique that can realize larger-capacity and higher-speed transmissions, when compared to conventional electrical wiring. In order to realize a large-capacity optical interconnection, silicon photonics is an essential component technology; the core materials are crystalline silicon (c-Si) and silicon dioxide. Silicon photonics is compatible with CMOS fabrication processes, and its high refractive-index contrast structures allow for a small footprint [1]. So far, a number of c-Si based devices such as low-loss wire waveguides, passive devices [2], and active devices including modulators exist [3], [4].

However, c-Si does not meet the requirements for some complex optical devices and systems because of its material properties. Unfortunately, c-Si has a poor luminescence property [5] and high optical nonlinearity [6]. In addition, it cannot be stacked as a multilayer owing to the high temperatures (of over 1000 °C) involved in deposition.

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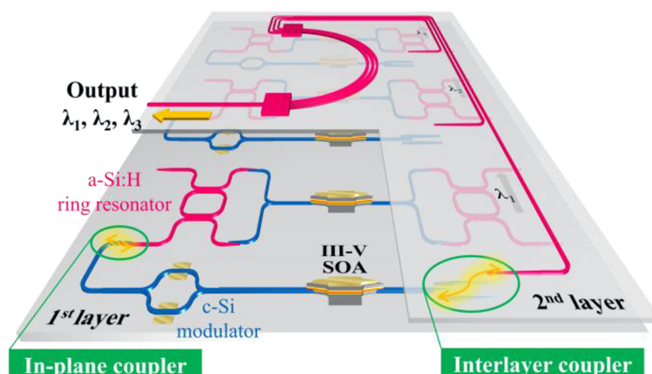

Fig. 1. Concept of WDM transmitter based on hybrid integration of III–V materials, c-Si, and a-Si:H.

In order to solve this problem, hybrid-material platforms have been widely studied. For example, an integration of III–V materials on Si [7]–[9] or Si/SiO_2/SiN platforms has been reported [10], [11] to overcome the disadvantages of c-Si.

Another approach is to use hydrogen-terminated amorphous Si (a-Si:H). Recent works show that the optical nonlinearity coefficient of a-Si:H can be changed from a high value to a low value, by changing its deposition conditions, in comparison with c-Si [12]–[14]. Using the highly nonlinear property of a-Si:H, efficient wavelength conversion via four-wave mixing in a relatively compact a-Si:H wire waveguide was demonstrated [15]. An important factor in the deposition is the temperature. a-Si:H can be deposited on Si at low temperatures (around 300 °C), with no damage to the underlying layers in the case of a back-end process. It is reported that a-Si:H can be stacked repeatedly and that it can realize multilayers easily for 3D optical integrated circuits because of this property [16]–[18].

There are still shortcomings for a-Si:H, such as the impossibility of current injection owing to low carrier mobility; this creates difficulties in realizing high-speed optical modulators or phase-change devices. Therefore, the integration of c-Si and a-Si:H as complementary materials provides various functions for an optical integrated circuit.

Fig. 1 shows a conceptual diagram of a wavelength-division-multiplexed (WDM) transmitter using the hybrid integration of III–V compound semiconductor materials, c-Si, and a-Si:H. Light is generated by a III–V and a-Si:H ring resonator and it is modulated by a c-Si modulator using current injection. Then, the signals are transmitted to a second a-Si:H layer by high-efficiency couplers between the stacked layers. Finally,

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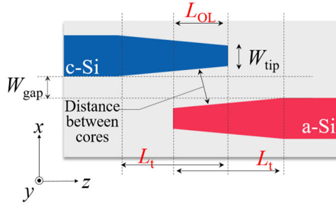

Fig. 2. Schematic of in-plane-type coupler.

TABLE I
PARAMETERS OF IN-PLANE-TYPE COUPLER

Parameter	Symbol	Range of value	Designed value
Taper length	L_t	0–100 μm	50 μm
Overlap length	L_{OL}	0–50 μm	25 μm
Tip width	W_{tip}	50–300 nm	150 nm
Gap width	W_{gap}	100–200 nm	150 nm

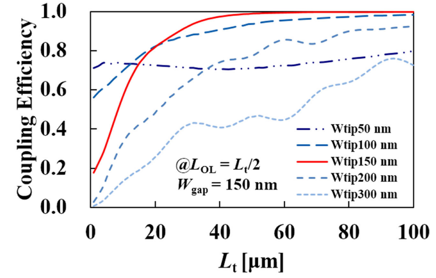

Fig. 3. L_t Dependence of coupling efficiency for each W_{tip}, when L_{OL} is set to $L_t/2$.

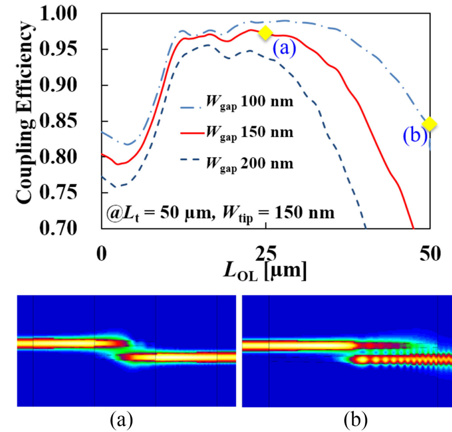

Fig. 4. L_{OL} Dependence of coupling efficiency for each W_{gap}, and its optical mode fields when (a) $L_{OL} = 25$ μm, and (b) $L_{OL} = 50$ μm.

the signals are gathered by arrayed waveguides and coupled to an optical fiber. It is reported that the power tends to concentrate at the ring resonators, which are located on both sides of the III–V material, causing nonlinearity in the core and worsening the lasing property [19]. This problem can be avoided by using a-Si:H with low nonlinearity as the ring resonator. Moreover, the second layer can be used actively, which increases the flexibility and reduces the circuit size.

A key component required for such hybrid devices is an efficient light-coupling device between the two waveguides of c-Si and a-Si:H. In this paper, we propose and demonstrate the in-plane and interlayer waveguide-type couplers for 2D/3D hybrid-material integration. In Section II, the in-plane-type couplers are described, and Section III describes the interlayer-type couplers. In each section, we explain the device design, fabrication process, and experimental results.

II. In-Plane-Type Coupler

Several reports describe the interlayer connections between different material waveguides [10], [11], [20], [21]. However, an in-plane connection has not yet been reported. Using different-material integration in the same layer, high integration density can be achieved.

A. Device Design

As a premise for the device design, it was assumed that a basic wire waveguide of c-Si (refractive index: 3.48) or a-Si:H (refractive index: 3.58) having a height of 220 nm and width of 450 nm was buried in SiO_2 (refractive index: 1.44). For these conditions, we designed structures with a wavelength of 1.55 μm operating in the TE mode using the Eigen mode expansion method and the finite-difference method.

One of the problems in designing couplers is the misalignment that occurs during electron beam lithography (EBL). The following discussion is based on the assumption that the controllable alignment accuracy in a state-of-the-art EBL and stepper is better than 50 nm [22].

The in-plane-type structure can be described with the help of Fig. 2. By introducing linear tapers into a directional coupler as described in [20], a coupler with a tolerance for variations in waveguide width and the refractive index of a-Si:H can be obtained. Table I shows the parameters of the in-plane-type coupler. In Fig. 2 and Table I, L_t and W_{tip} indicate the length and tip width of the taper, respectively. W_{gap} represents the gap width between the connected waveguides along the x-direction, and L_{OL} represents the overlapping length of the c-Si waveguide and the a-Si:H waveguide along the z-direction.

Initially, W_{gap} was set as 150 nm. Fig. 3 shows L_t dependence of coupling efficiency on for each W_{tip}, when L_{OL} is set to $L_t/2$. This relationship demonstrates that longer taper lengths correspond to higher coupling efficiencies. When L_t is longer than 50 μm, for a W_{tip} of 150 nm, more than 95% coupling efficiency is achieved. Wider W_{tip} show some fringes due to reflection, and narrower W_{tip} need longer taper lengths to attain the maximum coupling efficiency. Thus, from this figure, in order to yield a small footprint, a length of $L_t = 50$ μm and a width of $W_{tip} = 150$ nm are adopted in our experiments.

For this condition, Fig. 4 shows L_{OL} dependence of coupling efficiency for each W_{gap}. It was found that the coupling efficiency increases for smaller W_{gap}. From Fig. 4(a) and (b), when the phase is as shown in (a), a high coupling efficiency is achieved. In other cases, light cannot transit smoothly to the

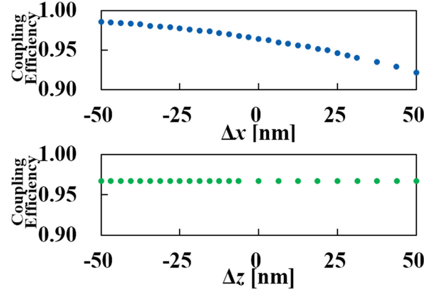

Fig. 5. Misalignment dependence of coupling efficiency for misalignments in x-direction (Δx) and z-direction (Δz).

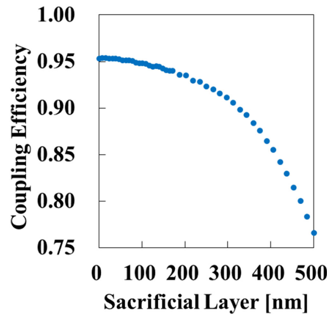

Fig. 6. Dependence of coupling efficiency on thickness of sacrificial layer for in-plane coupler.

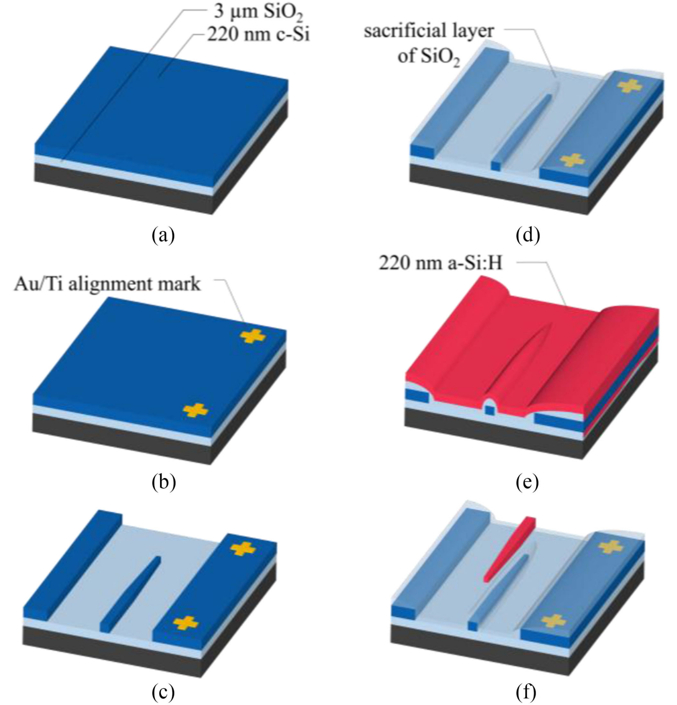

Fig. 7. Fabrication process of in-plane integration. (a) Initial wafer. (b) Fabrication of alignment mark. (c) Patterning c-Si waveguide. (d) Deposition of sacrificial layer. (e) Deposition of a-Si:H. (f) Patterning a-Si:H waveguide.

other waveguides and many reflections occur as shown in (b). While considering the distance between the cores (further discussion of which will be given in Section II-B), W_{gap} was set to 150 nm. At this time, the coupling efficiency was more than 95% in the range of $L_{\text{OL}} = 13 - 30\,\mu\text{m}$; hence, L_{OL} was set to $25\,\mu\text{m}$.

Fig. 5 shows the misalignment dependence of coupling efficiency. From this figure, it is observed that a high coupling efficiency of more than 90% is achievable for the presumed misalignment and change in index. In addition, by numerical analysis it is found that, when the thickness of a-Si:H changes by around 10%, the decrease in the coupling efficiency is less than 1%.

For in-plane integration, a sacrificial layer is required (further discussion on this is given in Section II-B). The sacrificial layer is a thin intermediate layer between the c-Si and a-Si:H layers, and is used as an etch-stop layer. Fig. 6 shows dependence of coupling efficiency on thickness of sacrificial layer. By this numerical analysis, a high coupling efficiency of more than 85% is maintained in the range of 0–400 nm of sacrificial layer despite the in-plane-type design. Moreover, considering the fabrication conditions (that are mentioned in the next section), the sacrificial layer thickness is set to 200 nm. For this value, a coupling efficiency of approximately 93% is attainable.

B. Fabrication

The in-plane integration can be realized by a three-step EBL process. The process flow is shown in Fig. 7. An essential part of this process flow is the deposition of a SiO_2 sacrificial layer. In order to cover a c-Si waveguide from an a-Si:H etching, a thin SiO_2 sacrificial layer must be introduced before the a-Si:H deposition.

First, on a silicon-on-insulator chip with a 220-nm-thick top silicon layer and a 3-μm-thick buried oxide layer (1), alignment marks were formed by EBL and metal evaporation (20-nm Ti/100-nm Au) (2). Next, a 700-nm thick ZEP520A-C_{60} resist [23] was spin-coated, and a c-Si waveguide was patterned by EBL and inductively-coupled-plasma–reactive-ion-etching with CF_4/SF_6 mixed gas (3). After that, SiO_2 was deposited as a sacrificial layer by plasma-enhanced chemical vapor deposition (PECVD) (4). Then, a 220-nm-thick a-Si:H was deposited using PECVD (5), and the a-Si:H waveguide was formed in the same way (6). Finally, SiO_2 was deposited as a cladding layer. Fig. 8(a) shows cross-sectional view of Fig. 7(5–6).

Fig. 8(b) shows a scanning electron microscope (SEM) image of the cross-sectional view of the c-Si waveguide after depositing a 200-nm sacrificial layer and a 220-nm layer of a-Si:H. After this, when the proceeding etching of 350 nm was conducted, the appropriate states shown in Fig. 8(c) were realized. As shown in Fig. 8(b), there is a stretch of upper layer (sacrificial layer and a-Si:H layer) on the c-Si waveguide. Thus, close attention must be paid to both the thickness of the sacrificial layer and the etching amount of the a-Si:H because there is the possibility that a-Si:H remains on the edge of the c-Si waveguide. If the etching amount is not sufficient, a-Si:H remains on parts of the edge of the c-Si waveguide as shown in Fig. 9(a). However, if the etching amount increases extremely (or the sacrificial layer is too thin), this results in the c-Si waveguide being

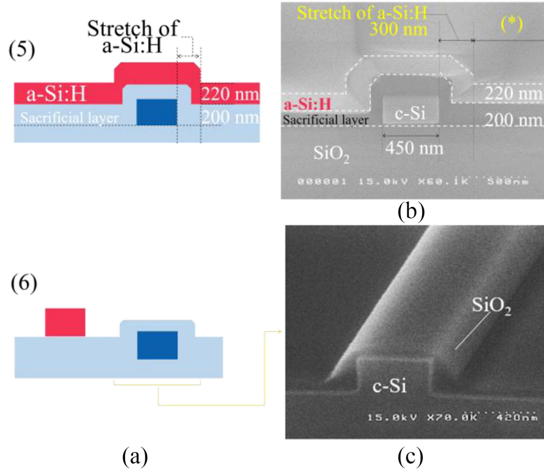

Fig. 8. (a) Cross-sectional view of Fig. 7 (5–6). (b) and (c) are the SEM views.

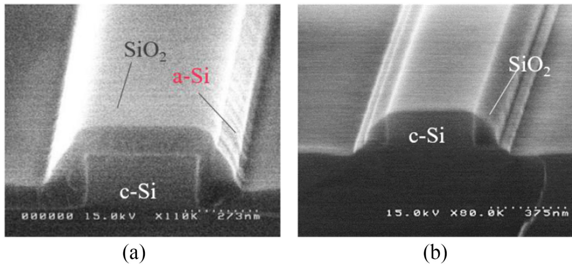

Fig. 9. Cross-sectional view of c-Si waveguide with sacrificial layer and a-Si:H, under improper conditions of (thickness of sacrificial layer, etching amount). (a) (150 nm, 220 nm). (b) (180 nm, 350 nm).

etched as shown in Fig. 9(b). In such a situation, there is a proper condition that the c-Si is covered with the sacrificial layer, and the a-Si:H does not remain as shown in Fig. 8(c). In this paper, as per such an appropriate condition, a 350-nm etching amount and 200-nm sacrificial layer thickness are adopted.

In this condition, the a-Si:H waveguide must be formed in the area depicted using the asterisk symbol (∗) in Fig. 8(b); hence, it is required that the a-Si:H waveguide is located 300 nm away from the c-Si waveguide. If the W_{gap} is 100 nm, then the distance between the cores will be 320 nm; if W_{gap} is 150 nm, then the distance between the cores will be 370 nm. Therefore, W_{gap} is set to 150 nm because $W_{\text{gap}} = 100\,\text{nm}$ (distance between cores = 320 nm) cannot be formed owing to a misalignment of ±50 nm.

Fig. 10 shows the cross-sectional view of the fabricated coupling region under this condition. It can be observed from this figure that, although undesired, a rib-waveguide shape is formed by the insufficient etching of the c-Si.

C. Measurement Results

The measurement system is illustrated in Fig. 11. An amplified spontaneous emission light source is used as the input power source. The light is TE-like polarized, using a polarizer and polarization controller, and is coupled to the device under test (DUT) by a lens-tipped single-mode fiber after passing through a polarization splitter. The light output from the DUT is coupled to an optical spectrum analyzer via an optical fiber.

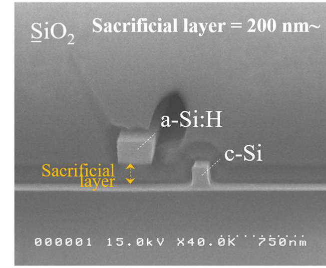

Fig. 10. Cross-sectional view of coupling region.

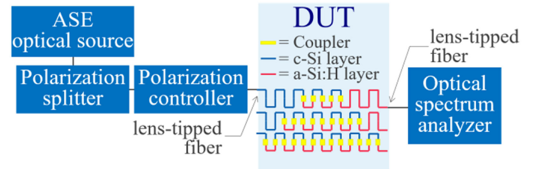

Fig. 11. Measurement system.

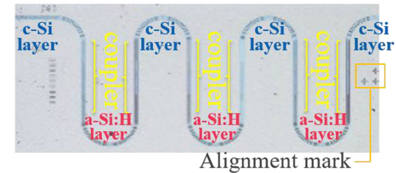

Fig. 12. Microscopic image of fabricated pattern.

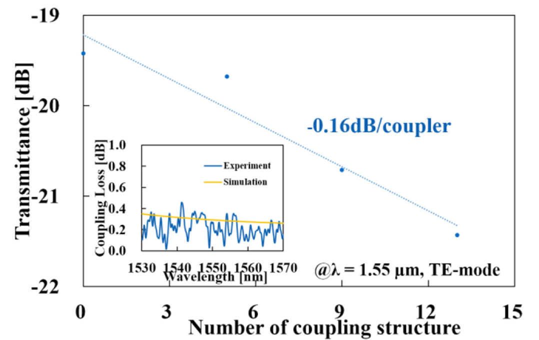

Fig. 13. Transmittance of in-plane-type coupler as a function of the number of coupling structures at λ of 1.55 μm (average power of 1548–1552 nm.) The inset shows the wavelength dependence of the coupling loss.

As shown in Figs. 11 and 12, the outline of the fabricated pattern is serpentine, and it has 5, 9, or 13 couples in the waveguides. In addition, because the pattern has a point symmetrical shape, the coupling efficiency of the coupler can be evaluated from the margins of the transmission losses of the waveguides, regardless of the waveguide loss.

Fig. 13 shows transmittance of in-plane-type coupler as a function of the number of coupling structures at λ of 1.55 μm. From this data, it can be seen that the in-plane-type coupler achieved a coupling efficiency (coupling loss) of 96.4%

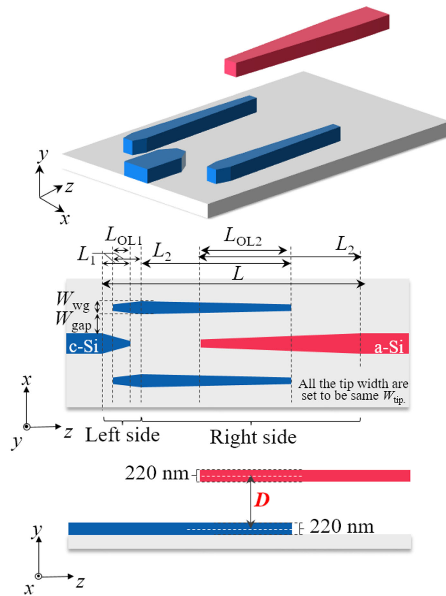

Fig. 14. Schematics of interlayer-type coupler.

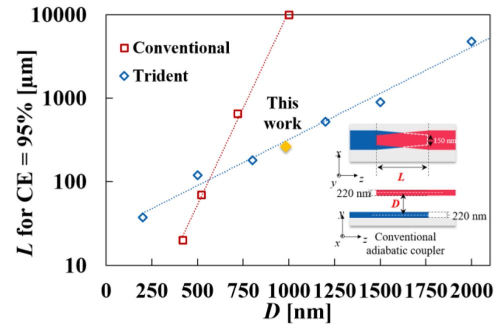

Fig. 15. Interlayer thickness dependence of device length for each vertical coupler.

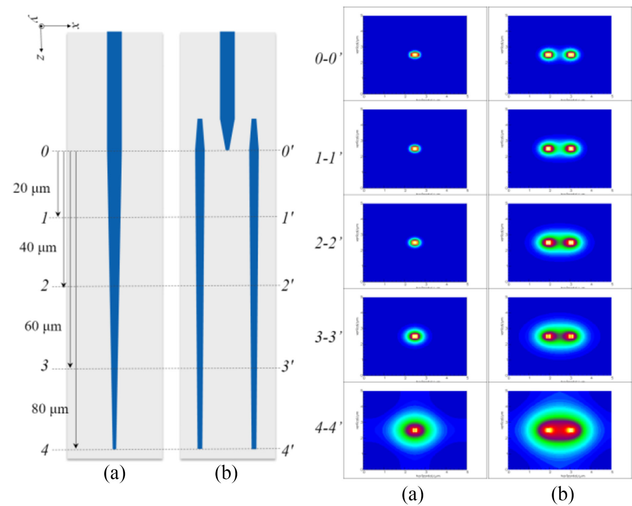

Fig. 16. Mode fields of (a) a single-tapered waveguide and (b) trident waveguide ($L_1 = L_{OL1} = 20\ \mu$m, $L_2 = 80\ \mu$m, $L_{OL2} = 40\ \mu$m, $W_{tip} = 150$ nm).

(−0.16 dB) per transition at a λ of 1.55 μm. In addition, the in-plane-type coupler shows an almost constant coupling loss of around 0.2 dB in the C-band region. It this experiment, anti-reflection coating was not applied for the facet of the waveguide; hence, the Fabry–Pérot resonance between the facets causes fine ripples.

A difference between the original design and the design in Fig. 10 is the rib-waveguide shape, which is caused by insufficient etching. However, numerical analyses reveal that the coupling efficiency does not vary (even when assuming a ∼20-nm rib). Thus, we conclude that the rib part does not influence the coupling property.

III. Interlayer-Type Coupler

A. Device Design

Two types of couplers have been reported as devices that can transmit light from layer to layer. One is a grating coupler, and the other is a directional coupler [11], [17], [18], [20], [21]. However, these couplers have trade-offs between the complexity of the device or the interlayer thickness. We proposed and demonstrated a high-efficiency grating coupler with a metal mirror that enables transmission with an arbitrary interlayer thickness—even with several μm of thickness [24]. However, this requires the accurate formation of grating; moreover, several of the mask processes include metal deposition. On the other hand, the directional-type coupler has a simple structure; hence, it can be fabricated easily and it can achieve a high coupling efficiency (but only at limited transmission distances such as several hundred nm). Reference [20] demonstrated a directional-type coupler with an interlayer thickness of 200 nm; however, this coupler caused interlayer crosstalk that could not be ignored. Another report describes a 600-nm interlayer and second-core concept [21], but then, the process flow becomes complicated. From the preceding discussion, a simple grating coupler structure using only Si and SiO_2 for μm-range transmissions may be attractive.

Towards this purpose, we propose a directional coupler with a trident structure as shown in Fig. 14; this coupler has a simple fabrication process, and it can be applied for interlayer transmissions across relatively long distances. The trident structures have parallel waveguides, which are located around two connected waveguides that taper. It is reported that a trident-type spot-size converter between wire waveguides and a laser diode exhibits high performance optical coupling and a high tolerance for misalignment [25]. In this work, we utilize this structure as an interlayer coupler.

Fig. 15 shows the interlayer thickness dependence on the device length for each vertical coupler. Although the conventional coupling structure, shown in [20], needs a 1-cm device length to achieve a coupling efficiency of 95%, in the case of an interlayer thickness of 1 μm, a device length of less than 400 μm is sufficient for the proposed trident coupler.

The reason for this is explained by Fig. 16. Fig. 16(a) and (b) shows the mode field profiles of a single-taper waveguide and trident waveguide, respectively. It is observed that the

TABLE II
PARAMETERS OF INTERLAYER-TYPE COUPLER

Parameter	Symbol	Range of value	Designed value
Taper length of left hand	L_1	0–20 μm	20 μm
Overlap length of left hand	L_{OL1}	0–20 μm	20 μm
Taper length of right hand	L_2	0–300 μm	200 μm
Overlap length of right hand	L_{OL2}	0–200 μm	125 μm
Tip width	W_{tip}	0–450 nm	150 nm
Gap width	W_{gap}	100–500 nm	200 nm
Width of the side waveguides	W_{wg}	250 nm (constant)	250 nm

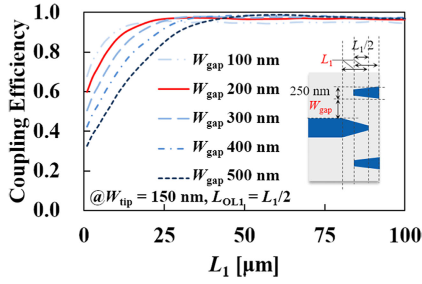

Fig. 17. L_1 dependence of coupling efficiency when overlap length L_{OL1} is $L_1/2$ for each W_{gap}.

trident waveguide realizes bigger mode fields than the single-taper waveguide of the same device length. As a result, we can expect the trident structure to use a shorter length to achieve a higher coupling efficiency when the interlayer distance is large.

This coupler is divided into a left side and right side, as shown in Fig. 14. The left side is designed first. Parameters of the interlayer-type coupler are shown in Table II. L_1 and L_2 indicate the taper lengths of the left hand and right hand sides, respectively, and L_{OL1} and L_{OL2} indicate the overlapping lengths of the left hand and right hand sides, respectively. W_{tip} signifies the tip width of the taper and W_{gap} signifies the gap width between the connected waveguides along the *x*-direction, as in the in-plane-type coupler. In this paper, W_{wg} indicates the width of the side waveguides and it is set to a constant value of 250 nm. Because the interlayer crosstalk is small enough to be ignored with an interlayer distance *D* of over 1 μm [16], *D* is set to 1 μm.

Fig. 17 shows the L_1 dependence on the coupling efficiency, when the overlap length L_{OL1} is $L_1/2$ for each W_{gap}. When L_1 is extended, the coupling efficiency is increased and a small W_{gap} provides a short taper length. During fabrication, a W_{gap} of less than 200 nm is difficult to form, so W_{gap} is set to 200 nm. Moreover, L_1 is set to 20 μm because a coupling efficiency of 95% is achieved for all $L_1 > 20$ μm. Under these conditions, L_{OL1} is varied in Fig. 18. In this figure, when L_{OL1} is set to 20 μm, the footprint of the left side is minimized, and a coupling efficiency of 95% is achieved; thus, L_{OL1} is set to 20 μm. The right side is designed in a similar fashion. Fig. 19(a) shows the L_2 dependence on the coupling efficiency when the overlap length L_{OL2} is L_2/2. This figure shows that the coupling efficiency is higher than 95% when $L_2 > 200$ μm. Thus, L_2 is set to 200 μm. Fig. 19(b) shows the L_{OL2} dependence when

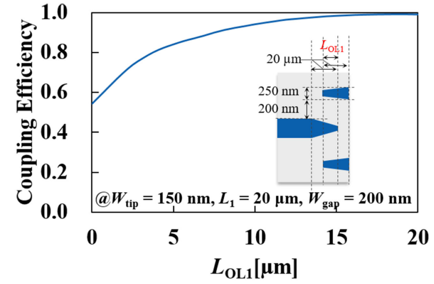

Fig. 18. L_{OL1} dependence of coupling efficiency.

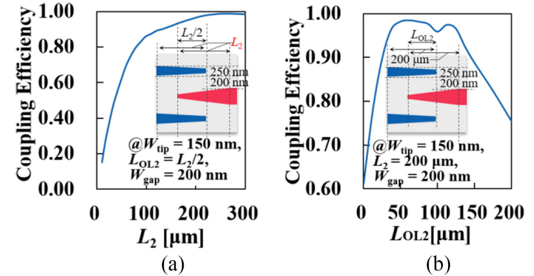

Fig. 19. (a) L_2 dependence of coupling efficiency when overlap length L_{OL2} is $L_2/2$, and (b) L_{OL2} dependence of coupling efficiency.

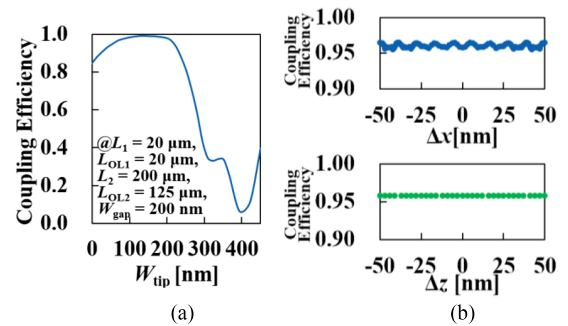

Fig. 20. (a) W_{tip} dependence of coupling efficiency in designed trident coupler, and (b) misalignment dependence of coupling efficiency for misalignments in *x*-direction (Δx) and *z*-direction (Δz).

$L_2 = 200$ μm. For a small footprint, L_{OL2} is set to 125 μm, and a coupling efficiency of 95% is achieved. Under this condition, W_{tip} is varied as shown in Fig. 20(a). From this figure, by deciding that $W_{\mathrm{tip}} = 150\,\mathrm{nm}$ even if W_{tip} varies by $\pm$50 nm, the coupling efficiency remains higher than 95%. Thus, W_{tip} is set to 150 nm. Finally, Fig. 20(b) shows misalignment dependence of coupling efficiency. It is indicated that a high coupling efficiency of more than 95% is achievable for the presumed misalignment and index variation. In addition, by numerical analysis it is found that, when the thickness of a-Si:H changes by around 10%, the decrease in coupling efficiency is less than 3.5%.

B. Fabrication

The process flow for the fabrication of the interlayer coupler is essentially identical to that of the in-plane coupler explained

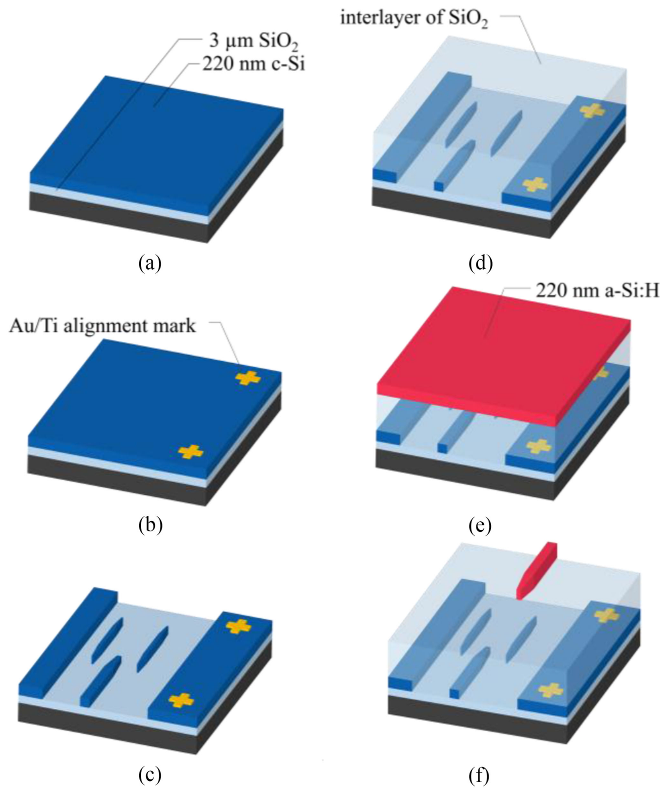

Fig. 21. Fabrication process for interlayer integration. (a) Initial wafer. (b) Fabrication of alignment mark. (c) Patterning c-Si waveguide. (d) Deposition of interlayer and CMP. (e) Deposition of a-Si:H. (f) Patterning a-Si:H waveguide.

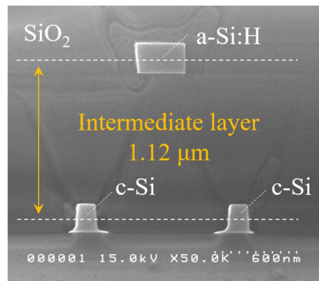

Fig. 22. Cross-sectional view of interlayer-type coupler.

in Fig. 7, except for the introduction of a chemical mechanical polishing (CMP) process to replace the sacrificial layer with an overetching condition. This process flow is shown in Fig. 21.

First, a wafer that has alignment marks and a c-Si pattern must be fabricated as shown in Fig. 21(1–3). Next, an interlayer of 1.5-μm-thick SiO_2 is deposited by PECVD and flattened by a CMP process to obtain a thickness of $1\ \mu$m, with the thickness controlled by an *ex situ* thickness monitor (4). Then, 220-nm-thick a-Si:H is deposited by PECVD (5), and an a-Si:H waveguide is formed in the same way (6). Finally, SiO_2 is deposited as a cladding layer.

Fig. 22 shows the cross section of the fabricated device. This figure confirms the fabrication of the parallel waveguides, but there are problems with the tails at the lower parts of the c-Si

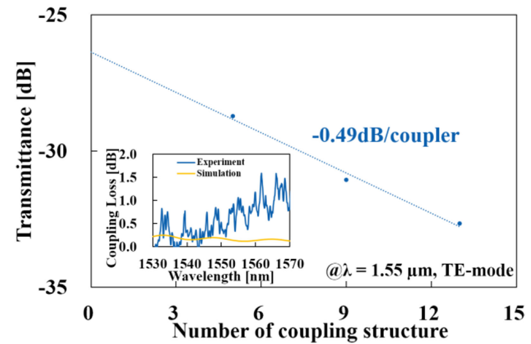

Fig. 23. Transmittance of interlayer-type coupler as a function of number of coupling structures at a λ of $1.55\ \mu\mathrm{m}$ (average power of 1548–1552 nm). Inset shows the wavelength dependence of coupling loss.

waveguides and with the thicker intermediate layer. The appearance of tails is a result of insufficient etching. The reason for this is the same as that in the in-plane-type coupler—the tails cause mode field shifts on the underside. In addition, the intermediate layer is 1.12-μm thick despite the intended design of 1 μm; this discrepancy is caused by an inaccuracy in the thickness measurement.

C. Measurement Result

The measurement system and the fabricated pattern are the same as that of the in-plane-type shown in Figs. 11 and 12. The coupling efficiency of the coupler is evaluated from the margins of the transmission losses of the waveguides, regardless of the waveguide loss.

Fig. 23 shows the number of coupling structures dependent on the optical transmission power. Based on this result, it can be inferred that the interlayer-type coupler achieves a coupling efficiency (coupling loss) of 89.3% (−0.49 dB) per transition.

In a simulation, when the intermediate layer thickness D was $1.12\ \mu$m, the coupling efficiency was 89.8%, which is in agreement with the measurement results. Thus, it is concluded that the main cause of the drop in coupling efficiency is the thicker intermediate layer. In the dependence of wavelength, the Fabry–Pérot resonance between facets causes fine ripples similar to those in the in-plane-type coupler. In addition, an increase in the coupling loss was observed at longer wavelengths. This may be due to the light leakage to the side Si-slab portion (we did not etch the whole Si layer, only a 5-μm trench was etched to save lithography time), since longer wavelengths have larger mode sizes.

IV. Conclusion

We demonstrated that the in-plane and interlayer-type couplers between c-Si and a-Si:H wire waveguides for 2D/3D hybrid-material integration were effective. The in-plane-type coupler realized stable coupling between two spaced waveguides by using a linear taper located at the tips of the waveguides. By introducing a trident structure, the interlayer-type coupler connected two waveguides efficiently with an interlayer distance of $1\ \mu$m via a simple structure. We applied an

in-plane-type process with a sacrificial layer, and a conventional interlayer-type process to these two couplers. Experimentally, the in-plane and interlayer-type couplers achieved coupling efficiencies of 96.4% (−0.16 dB) and 89.3% (−0.49 dB) per coupler, respectively. This result demonstrates the high performance of the waveguide-type couplers in terms of high coupling efficiency and high tolerance; thus, paving the way to develop hybrid integrated optical circuits.

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References

[1] B. Jalali and S. Fathpour, "Silicon photonics," in *Proc. IEEE Photon. Soc. 23rd Annu. Meeting.*, 2012, vol. 24, no. 12, pp. 489–489.

[2] T. Horikawa *et al.*, "Process control and monitoring in device fabrication for optical interconnection using silicon photonics technology," in *Proc. Int. Interconnect Technol. Conf. IEEE Mater. Adv. Metallization Conf.*, 2015, pp. 277–280.

[3] L. Liao *et al.*, "High speed silicon Mach–Zehnder modulator," *Opt. Express*, vol. 13, no. 8, pp. 3129–3135, 2005.

[4] D. J. Thomson *et al.*, "50-Gb/s silicon optical modulator," *IEEE Photon. Technol. Lett.*, vol. 24, no. 4, pp. 234–236, Feb. 2012.

[5] L. Vivien and L. Pavesi, *Handbook of Silicon Photonics*. London, U.K.: Taylor & Francis, 2013.

[6] Q. Lin, O. J. Painter, and G. P. Agrawal, "Nonlinear optical phenomena in silicon waveguides: Modeling and applications," *Opt. Express* vol. 15, no. 25, pp. 16604–16644, 2007.

[7] G. Roelkens, D. Van Thourhout, R. Baets, R. Nötzel, and M. Smit, "Laser emission and photodetection in an InP/InGaAsP layer integrated on and coupled to a silicon-on-insulator waveguide circuit," *Opt. Express*, vol. 14, no. 18, pp. 8154–8159, 2006.

[8] J. Van Campenhout *et al.*, "Electrically pumped InP-based microdisk lasers integrated with a nanophotonic silicon-on-insulator waveguide circuit," *Opt. Express*, vol. 15, no. 11, pp. 6744–6749, 2007.

[9] Y. Hayashi *et al.*, "Low threshold current density operation of a GaInAsP/Si hybrid laser prepared by low-temperature N_2 plasma activated bonding," *Jpn. J. Appl. Phys.*, vol. 52, no. 6R, p. 060202, 2013.

[10] J. F. Bauters *et al.*, "Silicon on ultra-low-loss waveguide photonic integration platform," *Opt. Express*, vol. 21, no. 1, pp. 544–555, 2013.

[11] M. Sodagar, R. Pourabolghasem, A. A. Eftekhar, and A. Adibi, "High-efficiency and wideband interlayer grating couplers in multilayer Si/SiO_2/SiN platform for 3D integration of optical functionalities," *Opt. Express*, vol. 22, no. 14, p. 16767, 2014.

[12] Y. Shoji *et al.*, "Ultrafast nonlinear effects in hydrogenated amorphous silicon wire waveguide," *Opt. Express*, vol. 18, no. 6, pp. 5668–5673, 2010.

[13] C. Grillet *et al.*, "Amorphous silicon nanowires combining high nonlinearity, FOM, and optical stability," *Opt. Express*, vol. 20, no. 20, pp. 22609–22615, 2012.

[14] C. Lacava *et al.*, "Nonlinear characterization of hydrogenated amorphous silicon waveguides and analysis of carrier dynamics," *Appl. Phys. Lett.*, vol. 103, no. 14, 2013, Art. no. 141103.

[15] C. Lacava *et al.*, "Ultra-compact amorphous silicon waveguide for wavelength conversion," *IEEE Photon. Technol. Lett.*, vol. 28, no. 4, pp. 410–413, Feb. 2015.

[16] J. Kang, N. Nishiyama, Y. Atsumi, T. Amemiya, and S. Arai, "Multistacked silicon wire waveguides and couplers toward 3D optical interconnects," *Proc. SPIE*, vol. 8630, pp. 863008–863012, 2013.

[17] J. Kang *et al.*, "Amorphous-silicon inter-layer grating couplers with metal mirrors toward 3-D interconnection," *IEEE J. Sel. Topics Quantum Electron.*, vol. 20, no. 4, pp. 317–322, Jul./Aug. 2014.

[18] J. Kang *et al.*, "50 Gbps data transmission through amorphous silicon interlayer grating couplers with metal mirrors," *Appl. Phys. Express*, vol. 032202, pp. 5–8, 2014.

[19] T. Kita, K. Nemoto, and H. Yamada, "Long external cavity Si photonic wavelength tunable laser diode," *Jpn. J. Appl. Phys.*, vol. 53, no. 4S, 2014, Art. no. 04EG04.

[20] R. Sun *et al.*, "Impedance matching vertical optical waveguide couplers for dense high index contrast circuits," *Opt. Express*, vol. 16, no. 16, pp. 11682–11690, 2008.

[21] R. Takei *et al.*, "Low-loss and low wavelength-dependence vertical interlayer transition for 3D silicon photonics," *Opt. Express*, vol. 23, no. 14, pp. 18602–18610, 2015.

[22] J. Kang *et al.*, "Layer-to-layer grating coupler based on hydrogenated amorphous silicon for three-dimensional optical circuits," *Jpn. J. Appl. Phys.*, vol. 51, 2012, Art. no. 120203.

[23] K. Inoue *et al.*, "Loss reduction of Si wire waveguide fabricated by edge-enhancement writing for electron beam lithography and reactive ion etching using double layered resist mask with C_{60s}," *Jpn. J. Appl. Phys.*, vol. 48, no. 3R, 2009, Art. no. 030208.

[24] Y. Kuno *et al.*, "Design of apodized hydrogenated amorphous silicon grating couplers with metal mirrors for inter-layer signal coupling: Toward three-dimensional optical interconnection," *Jpn. J. Appl. Phys.*, vol. 54, no. 4S, 2015, Art. no. 04DG04.

[25] N. Hatori *et al.*, "A hybrid integrated light source on a silicon platform using a trident spot-size converter," *J. Light. Technol.*, vol. 32, no. 7, pp. 1329–1336, Apr. 2014.

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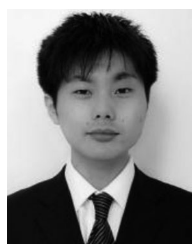

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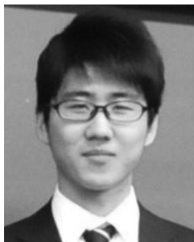

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