Performance Improvement of HfS_2 Transistors by Atomic Layer Deposition of HfO_2

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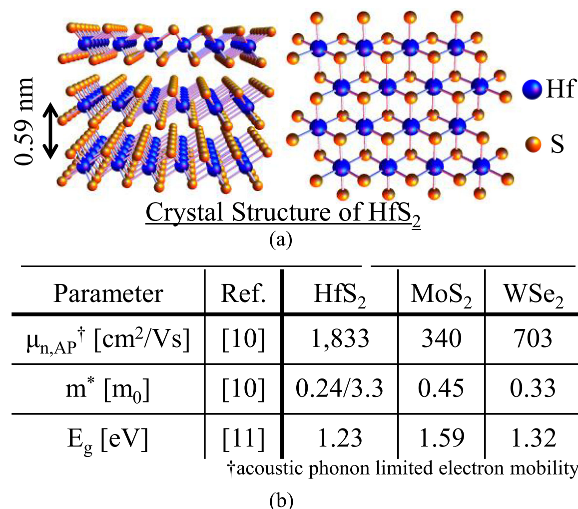
***Abstract*—Hafnium disulfide (HfS_2) is one of the transition metal dichalcogenides which is expected to have the high electron mobility and the finite bandgap. However, the fabrication process for HfS_2-based electron devices is not established, and it is required to bring out the superior transport properties of HfS_2. In this report, we have investigated the effects of the atomic layer deposited HfO_2 passivation on the current properties of HfS_2 transistors. HfO_2 passivation of the HfS_2 surface enhanced the drain current and significantly reduced the hysteresis. Moreover, HfO_2 passivation allows the use of a higher annealing temperature and further improvement of the drain current.**

***Index Terms*—MOSFETs, transition metal dichalcogenides, hafnium disulfide, atomic layer deposition.**

I. Introduction

The discovery of the graphene [1], [2] resulted in an enormous interest in the field of two-dimensional (2D) materials with atomic layer thickness. Graphene exhibits ultra-high mobility [3] with many other attractive properties and its device applications, such as transistors, photodetectors, and gas sensors have been widely studied. However, the zero bandgap in graphene makes it difficult to suppress the off leakage current of metal-oxide-semiconductor field-effect transistors (MOSFETs) [4], which is one of the most important performance parameters for low-power logic applications. Therefore, in recent years, various types of transition metal dichalcogenides (TMDs), such as MoS_2 [5], [6], WS_2 [7], and WSe_2 [8], have been investigated as post-graphene 2D materials for extremely scaled low power and high-speed logic applications. These TMDs have both the finite bandgap and extremely thin layer structure (<1 nm), which is attractive for MOSFETs with a channel length less than 10 nm.



Parameter	Ref.	HfS_2	MoS_2	WSe_2
$\mu_{n,AP}^{\dagger}$ [cm^2/Vs]	[10]	1,833	340	703
m^* [m_0]	[10]	0.24/3.3	0.45	0.33
E_g [eV]	[11]	1.23	1.59	1.32

†acoustic phonon limited electron mobility

(b)

Fig. 1. (a) Crystal structure and (b) fundamental electrical properties of HfS_2.

Hafnium disulfide (HfS_2) is a semiconducting TMD, which has a 2D crystal structure with octahedral coordination and the single layer thickness of 0.59 nm [9]. HfS_2 is expected to exhibit high acoustic phonon limited electron mobility (~1,800 cm^2/Vs) [10] and adequate bandgap (~1.2 eV) [11] as shown in Fig. 1.

In our previous studies, we demonstrated the device operation of few-layer HfS_2 MOSFETs with robust current saturation and good on/off ratio [12], [13]. Some other groups also reported on HfS_2 applications based on theoretical calculations [14], device fabrication [15]–[17], and crystal growth [18]. However, the maximum drain current of the reported HfS_2 FETs is only several hundreds of nA/μm or less because the fabrication process for HfS_2 MOSFETs remains to be established. In addition, in several cases, large hysteresis and severe instability of drain current against measurement sequences were observed in the atmosphere owing to charge traps. Moreover, time-dependent degradation of FET current in air with high humidity simultaneously appeared. Atmospheric degradation is one of the critical issues in the realization of high performance HfS_2 FETs and the evaluation of material properties. The degradation seems to be caused by the reaction between the HfS_2 surface and moisture, oxygen and other contaminants in air. To prevent this degradation and instability, the surface of the 2D material should be passivated and isolated from the atmosphere [16] to reduce the

Manuscript received September 30, 2016; accepted January 21, 2017. Date of publication January 31, 2017; date of current version July 7, 2017. This work was supported by the Japan Society for the Promotion of Science KAKENHI under Grant JP16H00905. The review of this paper was arranged by Associate Editor NANO2016 Guest Editors.

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Digital Object Identifier 10.1109/TNANO.2017.2661403

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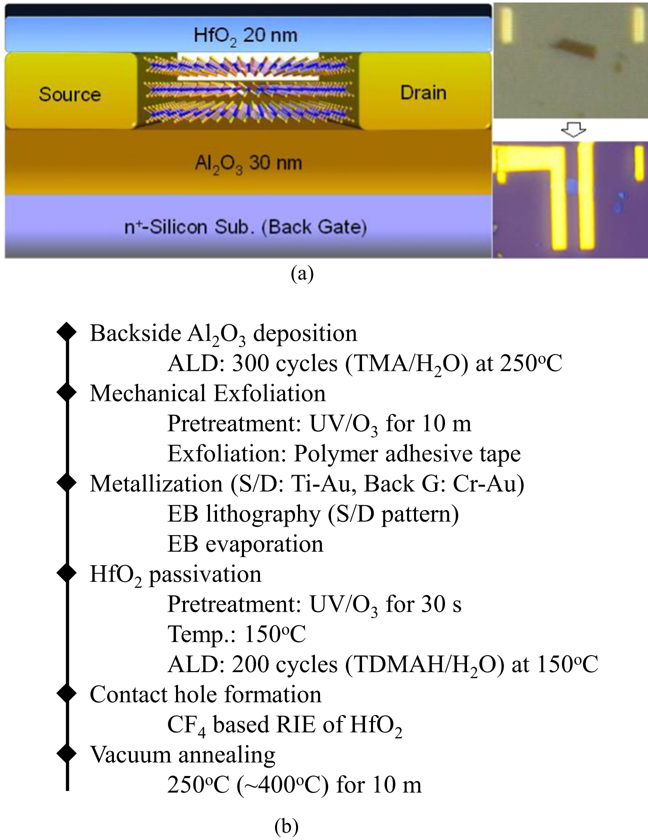


Fig. 2. (a) Schematic image of the device structure of HfS$_2$ back-gate FET with HfO$_2$ passivation and optical images of after exfoliation and after HfO2 passivation. (b) Fabrication process flow. (a) Device structure (b) Fabrication process.

trap states and absorption of gas atoms, respectively. Previously, we attempted to protect the surface by PMMA spin-coated on HfS$_2$ FET [19]. Although it indicated some improvement in current performance, the protection using PMMA was not robust enough to protect the surface from atmospheric degradation for longer duration.

In this report, we investigate the effects of surface passivation by atomic layer deposition (ALD) of the HfO$_2$ dielectric, which is commonly used as a high-k gate insulator in MOSFETs. A significant reduction of hysteresis was obtained compared to bare devices measured in the atmosphere. Additional annealing after HfO$_2$ passivation enhances the device performance of HfS$_2$ FETs and a maximum drain current of 4 μA/μm was observed, which is higher than all reported values for the HfS$_2$ channel with solid gate dielectrics.

II. Device Structure and Fabrication

Fig. 2 shows the schematic of the fabricated device structure along with the optical microscope images of the HfS$_2$ flake after exfoliation and the completed device structure, which is covered by HfO$_2$. The HfO$_2$ cap layer resulted in a change in the color of flakes and back-gate insulator. Multilayer HfS$_2$ is used as the channel of the MOSFETs. Although the number of layers was not directly measured in this study, the thickness may be approximately 4-6 layers (2.4-3.6 nm); this was estimated based on the color, brightness, and contrast compared with those from previous studies. An HfO$_2$ passivation layer was deposited to encapsulate the channel and contacts. Gate bias was applied from the degenerately n-doped Si substrate as the back gate through the Al$_2$O$_3$.

The fabrication process of MOSFETs based on mechanical exfoliation is as follows. First, the back-gate Al$_2$O$_3$ insulator is fabricated by performing 300 cycles of ALD (around 30 nm thick) on the n$^+$-Si substrate at 300 °C with trimethylaluminum (TMA) and water as precursors. Second, HfS$_2$ flakes were transferred to the substrate by micromechanical exfoliation using polymer adhesive tape; this was accomplished by the pre-treatment of the oxide surface by UV/ozone cleaner for 10 m to remove the hydrocarbon-based contamination and facilitate the contact between HfS$_2$ and Al$_2$O$_3$. Source/drain (S/D) electrodes and back gate contact were fabricated by electron beam (EB) lithography (only for S/D) and EB evaporation of Ti 20 nm/Au 60 nm and Cr 20 nm/Au 100 nm, respectively. Many reports discuss the difficulty and mechanism of ALD on 2D materials [20]–[22], and they suggest the solutions such as UV/O$_3$ functionalization [23] or introduction of buffer layers [17], [24], [25]. Third, the surfaces of the HfS$_2$ flakes were pretreated by UV/Ozone for 30 s, to clean up the resist residue from the surface with the partial oxidation of HfS$_2$. The self-limiting layer-by-layer oxidation of TMD was reported for WSe$_2$ [26]. In the case of HfS$_2$, there is a possibility of the formation of HfO$_x$ layer on HfS$_2$ with the sacrifice of few surface layers. If the assumption is correct, the ozone-treated HfS$_2$ surface has the seed layer, which may be suitable for the ALD of HfO$_2$. After a long exposure to ozone (e.g. 10 m), the conductivity of the few-layered HfS$_2$ almost vanished owing to the full oxidation of the HfS$_2$ layers. On the other hand, the effects of 30 s UV/O$_3$ treatment on $I_D - V_{GS}$ characteristics were negligible or slight in the measurement of bare HfS$_2$ devices (not shown). The samples were then loaded into the ALD chamber and encapsulated by HfO$_2$ at 150 °C using the precursors of Tetrakis(dimethylamino)Hafnium (TDMAH) and H$_2$O for 200 cycles. The contact holes to S/D electrodes were formed by CF$_4$ reactive ion etching of HfO$_2$ with the etching mask of PMMA patterned by EB lithography. Finally, vacuum annealing was carried out at 250 °C for 10 min to improve the HfS$_2$/HfO$_2$ interface and contact properties. The fabricated devices were measured in atmosphere using the semiconductor parameter analyzer.

III. Reduction of Hysteresis

Fig. 3 indicates the transfer characteristics of the bare (black) and passivated (red) HfS$_2$ MOFETs with similar back gate structures (30-nm-thick Al$_2$O$_3$/Si) in (a) linear and (b) semi-log plots. The inset SEM image in (a) is the measured sample for the passivated device. The channel length L_{ch} and width W_{ch} were estimated to be 2 μm. In the case of the bare device, L_{ch} was the same as that of the passivated device. Although W_{ch} was different for the two devices, all properties were normalized by W_{ch}.

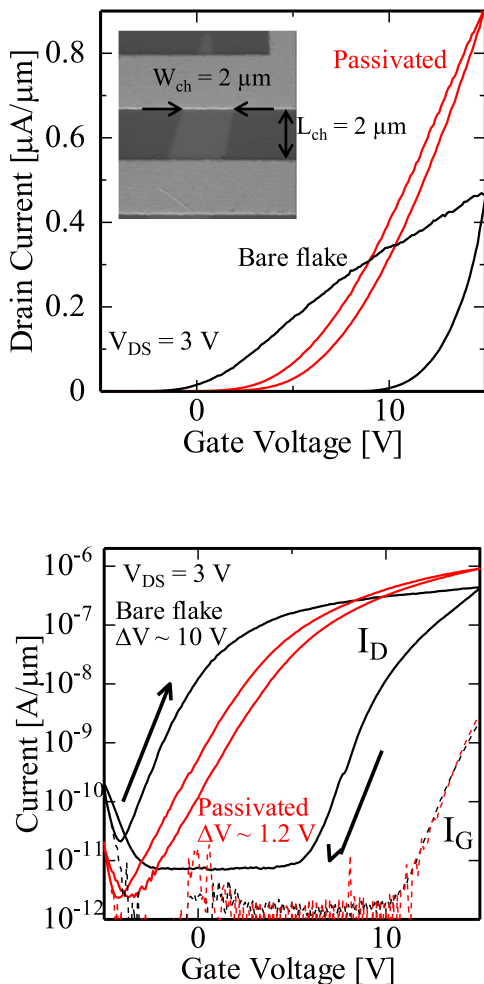


Fig. 3. Comparison of the hysteresis of the transfer curves between bare and HfO_2 passivated HfS_2 MOSFETs. (a) Transfer characteristics in linear plot (b) Transfer characteristics in semi-log plot.

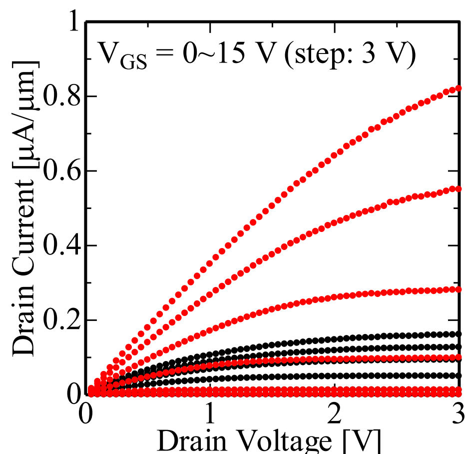


Fig. 4. Output characteristics of HfO_2 passivated MOSFET.

The maximum drain current at $V_{DS} = 3$ V and $V_{GS} = 15$ V was 0.9 μA/μm for the passivated device. Although the drain current for many devices obtained by the passivation process showed a trend of being higher than the bare HfS_2, the effect of passivation on the enhancement of the drain current is not yet clear owing to process fluctuation. The threshold voltage of the HfS_2 FET was over 0 V, and the enhancement mode n-type carrier transport was observed.

A typical bare HfS_2 sample, which was exposed to air during the measurement, showed a significant voltage shift ΔV of around 10 V between the forward and backward sweep in the hysteresis measurement. In contrast, the HfO_2 passivated device fabricated in this study showed a suppressed ΔV of less than 1.2 V. This significant reduction in hysteresis by surface passivation suggests that the greater part of the charge trapping occurred on the outermost surface of the HfS_2 flake. The trap state densities simply estimated by the hysteresis ΔV and oxide capacitance were over 10^{13} cm^{-2} for the bare sample and less than 2×10^{12} cm^{-2} for the passivated sample. The remaining trap charges in the passivated device existed at the interface between HfS_2 and Al_2O_3 or in bulk Al_2O_3. For further reduction of trap charges, the development of the back-gate insulator and surface treatment before mechanical exfoliation, and the improvement of the interface after transfer should be investigated.

The gate leakage current of the fabricated devices is simultaneously plotted in Fig. 3(b). Under strong bias ($V_{GS} < -3$ V or $V_{GS} > 10$ V), the gate current increased exponentially. This gate leakage current and breakdown of the insulator could occur between the S/D pad and the n^+-Si back gate, and it limits the maximum drain current through the allowable gate voltage. The increase in the drain current observed at the back bias region ($V_{GS} < -3$ V) is almost similar to the gate leakage curve and it does not indicate hole conduction. Particularly in the passivated device, the gate leakage floor seems to limit the observable on/off ratio. The improvement in the quality of ALD Al_2O_3 will be required for not only the reduction of charge traps but also superior insulating properties.

Fig. 4 shows the output characteristics of the HfO_2 passivated device. Robust current saturation behaviors were observed for both devices, with and without passivation. The drain current at $V_{DS} = 3$ V and $V_{GS} = 15$ V was around 0.82 μA/μm for the passivated device and 0.16 μA/μm for the bare device. The difference of drain current between the transfer and output characteristics with the same bias condition was around 10%. It was contrary to bare devices, which shows over a two times difference between the transfer and output measurement. This mismatch of the drain current, which depends on the bias history, also indicates high-density trap states.

Moreover, the time-dependent degradation of the drain current in the atmosphere was prevented by the HfO_2 capping. One month after the exfoliation and HfO_2 deposition, many devices indicated the drain current density of sub-microampere or a few microampere/μm without a severe decrease, in contrast to the bare devices [19]. Therefore, the ALD of HfO_2 seems to provide good protection from the oxidation and absorption of several types of contaminants from the atmosphere.

IV. Vacuum Annealing of HfO_2 Passivated FET

Previously, we reported the current enhancement of HfS_2 FET using vacuum annealing to remove surface contaminants and

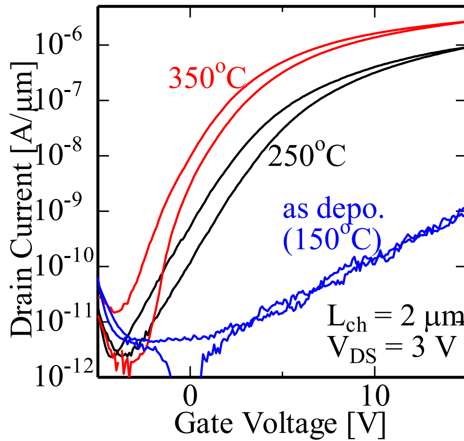
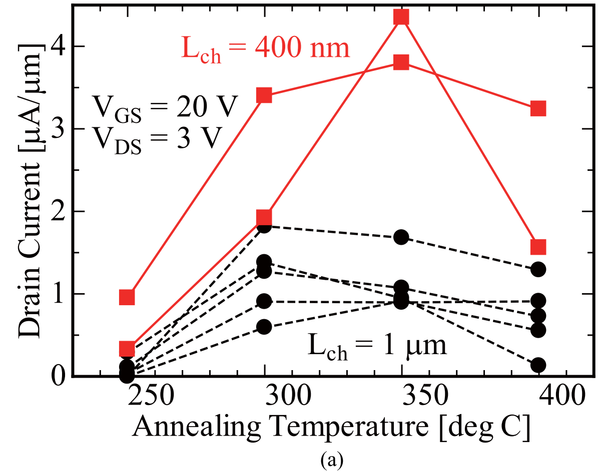


Fig. 5. Effects of vacuum annealing on $I_D - V_{GS}$ characteristics of HfO_2 passivated HfS_2 MOSFET.

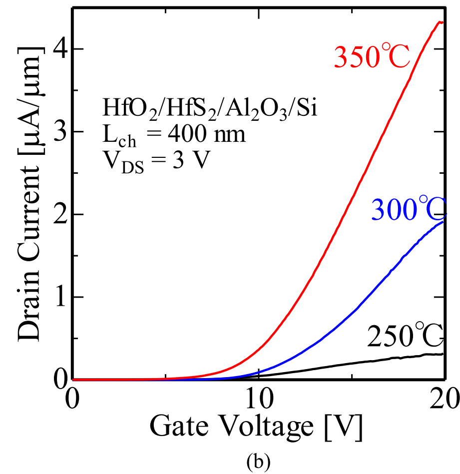
reduce contact resistance between Ti and HfS_2 [19]. In the case of the bare HfS_2, the optimum annealing temperature was estimated to be 250 °C. At an annealing temperature of 350 °C, the device performance degraded severely. This degradation may be caused by the removal of S atoms from the surface and the formation of a disordered crystal structure. According to that result, the annealing temperatures of both the bare and passivated samples discussed in Section III were set at 250 °C. Capping layers could allow higher tolerance because the top insulator prevents the movement of atoms. Therefore, we reinvestigated the effect of vacuum annealing for the HfO_2 passivated devices.

Fig. 5 shows the effects of vacuum annealing on the $I_D - V_{GS}$ characteristics of the HfO_2 covered HfS_2 FET. Three curves were observed for the same device. The first I−V measurement was carried out after HfO_2 deposition and the formation of contact holes. The "as deposited" device in this experiment was exposed to annealing at 150 °C for approximately 1 h in Ar ambient through the deposition process in the ALD chamber. The gate modulation of the drain current of the "as deposited" device was quite small with a maximum drain current of only 1 nA/μm and an on/off ratio of 100. Next, the sample was annealed at 250 °C for 10 m in a vacuum tube furnace. The drain current was significantly increased (0.9 μA/μm) by the annealing as shown in the above section and mentioned in our previous report for bare HfS_2. Then, the additional annealing was performed again at 350 °C. Further increase of the drain current to 2 μA/μm and current slope in the subthreshold region were obtained compared to 250 °C. The hysteresis was also reduced slightly except for the very low current region, which was affected by the gate leakage properties. From these results, the effects of annealing are expected to decrease the contact resistance and achieve a better quality interface. Thus, HfO_2 capped HfS_2 indicated the improvement of current properties by higher temperature annealing at 350 °C.

For a detailed investigation of the optimum annealing temperature, some devices fabricated on a 40-nm-thick Al_2O_3 were measured with different annealing temperature of 250, 300, 350, and 400 °C. Fig. 6(a) plots the drain current at $V_{DS} = 3$ V and $V_{GS} = 20$ V for six devices. All devices showed a clear current



(a)



(b)

Fig. 6. (a) Annealing temperature dependence of the drain current at $V_{GS} =$ 20 V and V_{DS} of 3 V for several devices with the two types of channel length L_{ch}. (b) $I_D - V_{GS}$ characteristics of the HfO_2 passivated HfS_2 transistor with different annealing temperature of 250, 300, and 350 °C for the same sample. (a) Comparison for several devices (b) Transfer characteristics.

increase with a increase in the annealing temperature from 250 to 300 °C. On the other hand, from 300 to 350 °C, half of the samples indicated enhancement and the others showed diminishment. At the annealing temperature of 400 °C, the drain current deteriorated for almost all devices. Therefore, the annealing temperature of HfO_2 capped HfS_2 should be set between 300 and 350 °C. This optimum range of annealing temperature might be caused by two different phenomena effects in HfS_2 FET as mentioned below. The high temperature may improve the interface of Ti/HfS_2 (S/D contact) and HfS_2/Al_2O_3. However, it also has a possibility to harm HfS_2 itself or cause the diffusion of metal atoms into HfS_2.

Fig. 6(b) describes the annealing temperature dependent transfer curves for one device, which shows the highest drain current in this experiment. The maximum drain current of 4.3 μA/μm was accomplished with an annealing temperature of 350 °C. The drain current was higher than the values in previous reports about HfS_2 FET with a solid gate structure [12], [13], [16]–[19]. The extracted effective mobility was less than 1 cm^2/Vs for this device. It was comparable to our previous works. All HfS_2 FETs have not resulted in expected

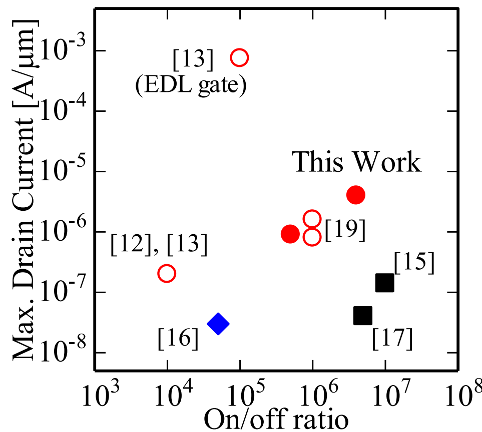


Fig. 7. Benchmarking of the device performance of HfS_2 FETs in previous reports. All dots plot the maximum drain current for each bias condition and on/off ratio between the maximum and minimum drain current.

high mobility yet as there are many factors that limit mobility; for example, impurity scattering, contact resistance, interface quality, and additional scattering processes [27].

Fig. 7 describes the benchmarking of HfS_2 FET focused on the maximum drain current and on/off ratio. The HfO_2 passivation and vacuum annealing discussed in this paper contributed in improving the drain current. However, its value was still $\sim$100 times smaller than the HfS_2 FET with electric double layer gate structure [13] and other matured layered materials (e.g., MoS_2 [28], Phosphorene [29]). Further development of the fabrication process and the investigation of physical properties are required to achieve high performance with an HfS_2 system.

V. Conclusion

We investigated the effect of surface passivation for HfS_2 MOSFETs using ALD HfO_2, to improve the stability of the I-V characteristics. The maximum drain current of 0.9 μA/μm was observed at $V_{DS} = 3$ V and $V_{GS} = 15$ V. The hysteresis width ΔV decreased apparently by the passivation from 10 V to 1.2 V. The protection of the surface by the high-k insulator is an efficient way to reduce the trap charges and improve stability. The vacuum annealing at 300-350 °C improved the drain current to 4.3 μA/μm for HfO_2 capped HfS_2 FET.

Acknowledgment

The author would like to thank Associate Prof. K. Nagashio for the helpful discussions and comments and Mr. S. Tamura for the technical support with the EB lithography.

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