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20 Gbps operation of membrane-based GaInAs/InP waveguide-type p–i–n photodiode bonded on Si substrate

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A GaInAs/InP waveguide-type p–i–n membrane photodetector is shown to be a strong candidate for on-chip optical interconnection. A responsivity of 0.95 A/W is estimated for a device length of 30 µm. The 3 dB cutoff frequency is measured to be 13.3 GHz at a reverse bias of 3 V, which is in good agreement with the observed clear eye opening pattern up to 20 Gbps for a non-return-to-zero signal. Moreover, a bit error rate of less than 1×10^{-9} is obtained at data rates of 20 and 10 Gbps with input powers of −10 and −13 dBm, respectively.
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In recent years, on-chip optical interconnection has attracted considerable attention globally owing to its significant potential for overcoming the fundamental limitations of electrical interconnects, such as signal delay and Joule heat generation in the wire layer of large-scale integrated (LSI) chips.[1,2] Ultralow-power-consumption on-chip photonic integrated circuits consisting of optical devices with small footprints are urgently required for this approach to remain competitive with electrical interconnects developed in the near future.[3] A membrane-structure-based in-plane photonic platform has been proposed to fulfill this demand.[4,5] The membrane structure consists of a thin semiconductor core layer sandwiched by low-refractive-index dielectric materials, such as air, SiO_2, or benzocyclobutene (BCB), which can provide significantly strong optical confinement to the active region of a laser source or the absorption region of a waveguide-type photodetector (PD), leading to miniaturized devices with low energy cost. In this case, a lateral p–i–n structure is required for electrical pumping and photocurrent collection.[6,7] Specifically, for a PD, the power consumption can be reduced significantly by replacing the transimpedance amplifiers (TIAs) and post amplifiers (PAs), which are commonly used in optical receiver systems, with a directly connected large load resistance.[8,9] Such a receiver-less PD can provide sufficient output voltage to drive the subsequent electrical circuit without excessive energy cost of the amplifiers. The power consumption of the entire optical link can be further reduced because the thermal noise generated in the PD will be decreased. Thus, the output required from the laser diode will be lower owing to the improved sensitivity. In this case, the device capacitance, that is, the device size, should be extremely small to maintain the resistance-capacitance constant. Therefore, the membrane-based PD is considered a strong candidate for on-chip optical interconnection.

In a previous study,[10] we proposed a lateral p–i–n waveguide-type PD based on a GaInAsP/InP multiple quantum well (MQW) absorption layer on a semi-insulating (SI) InP substrate. Despite its large absorber length and absorber width, its responsivity was measured to be less than 0.3 A/W owing to both the low absorption efficiency of the MQW structure with regard to its band gap wavelength (around 1.55 µm) and the weak optical confinement to the absorber. Subsequently, the PD was improved by replacing the MQW structure with a GaInAs bulk absorber.[11] The absorber volume is reduced owing to the larger material absorption coefficient of GaInAs. Nevertheless, leakage of the input light into the bottom SI-InP substrate remains an obstacle to increasing the responsivity. Recently, a membrane-based MQW PD formed on a Si substrate was reported as a component of a monolithic integrated circuit in which the SI-InP substrate is replaced with a SiO_2 bottom cladding layer, which enhances the vertical optical confinement to the absorber, thereby increasing the responsivity to 0.8 A/W at a similar absorption length of 200 µm compared to previously reported devices.[12] In the latest report, we introduced only the static characteristics of a membrane-based GaInAs bulk waveguide-type PD.[13]

In this work, we demonstrate the mentioned membrane-based GaInAs bulk waveguide-type PD with an even greater responsivity of 0.95 A/W and an extremely small device length of 30 µm. Its high-speed operation, including both small-signal and large-signal responses, is evaluated. The 3 dB cutoff frequency is measured to be 13.3 GHz at a reverse bias of 3 V, which is significantly higher than that of the previously developed membrane-based MQW PD. A schematic of the GaInAs/InP p–i–n waveguide-type membrane-based PD bonded on a Si substrate is shown in Fig. 1. A 30-µm-long absorption section with a 120-nm-thick GaInAs bulk layer is connected to a 155-nm-thick GaInAsP (λ_g = 1.22 µm)-core-layer passive waveguide region using a butt-jointed built-in (BJB) structure. The fabrication process was very similar to that previously reported except for the introduction of the GaInAs bulk absorption layer instead of the MQW layer.[12] It was confirmed that the GaInAs bulk and GaInAsP core have the same stripe width W_s of 0.7 µm.

Figure 2(a) shows the responsivity of the fabricated PD with a fixed wavelength of 1.55 µm under different bias voltage conditions. The transverse-electric-polarized light from the lensed fiber is input to the PD through the GaInAsP waveguide. The facet of the passive waveguide is formed by cleavage with no coating. In consideration of the fiber–chip coupling efficiency, which is calculated to be approximately 20% according to the finite difference method (FDM), the responsivity is estimated to be 0.95 A/W. This improvement in the responsivity within this extremely small absorption length can be attributed to not only the large absorption coefficient of GaInAs but also the high coupling efficiency of the BJB structure. According to the calculation result based on the FDM, a coupling efficiency exceeding 95% and a

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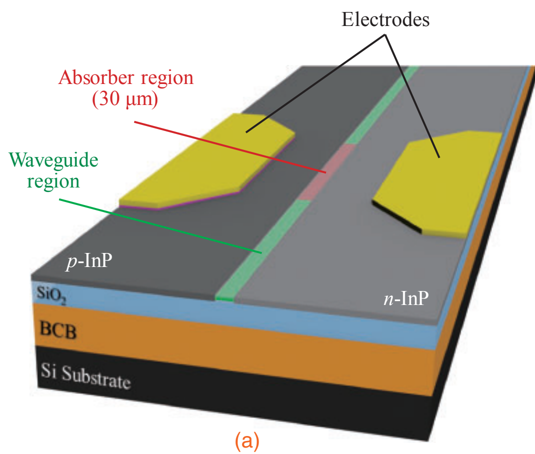
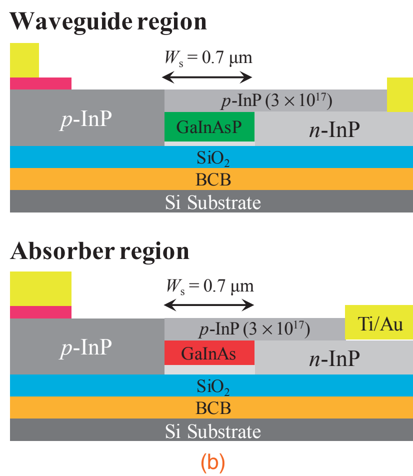


(a)



(b)

Fig. 1. Schematics of (a) structure and (b) cross-sectional structures of membrane-based GaInAs p–i–n PD.

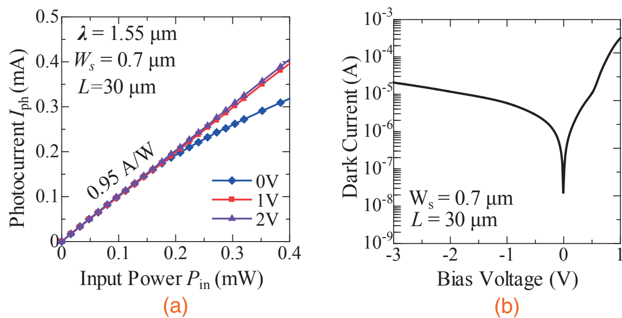


Fig. 2. (a) Responsivity and (b) dark current at different bias voltages.

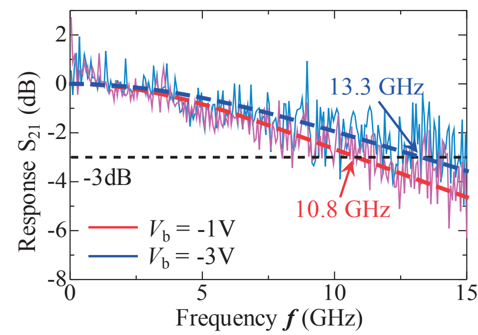


Fig. 3. Cut-off frequency at different bias voltages. Solid line: measured data; dashed line: fitting data based on LMS.

reflectivity of less than −40 dB can be obtained using this BJB structure. Such good coupling can be attributed to the extremely small differences in both the effective refractive index and the modal field distribution between the passive waveguide and the absorber region. Owing to the compact absorber region, saturation of the photocurrent caused by hole accumulation is observed under a bias condition of 0 V when the input light power exceeds 0.2 mW. However, it is considered that sufficient linearity has been obtained because the required received power from the laser diode is usually below 100 μW for realizing an ultralow-power-consumption optical interconnection, the energy cost of which is expected to be less than 100 fJ/bit or even 10 fJ/bit at a data rate of more than 10 Gbps. The dark current characteristic of the measured membrane photodiode is shown in Fig. 2(b). The dark current of this PD ranges from 5.7 to 20.6 μA as the reverse bias voltage increases from −1 to −3 V, which is much larger than the value for the previously reported MQW-absorber-based PD. This unremarkable dark current might be attributed to the crystal quality of the *u*-GaInAs or the saturation current caused by the pn junction region (top *p*-InP cladding and side *n*-InP cladding), as shown in Fig. 2(b). Alternatively, the other most likely reason is surface recombination of generated carriers trapped at the hetero interface. Fine adjustment of the fabrication conditions might be required to obtain better epitaxial regrowth.

Figure 3 shows the small-signal response S_{21} of the fabricated device under bias voltages of −1 and −3 V. The measurement is carried out using a vector network analyzer (VNA), which provides an electrical signal that drives a lithium niobate (LN) modulator after response calibration. The modulated light from a tunable laser through the LN modulator is incident on the PD. The solid and dashed lines represent the measured data and the fitting curve based on the least mean squares (LMS) method, respectively. The 3 dB bandwidth is found to be 10.8 and 13.3 GHz at bias voltages of −1 and −3 V, respectively. Vibration of the measured frequency response can be attributed to an induced error caused by changing of the cable connection after calibration and the weak signal output from the photodiode due to the small incident light power (which is limited by the maximum power for the external light source), the large insertion loss of the LN modulator, and the low fiber–chip coupling efficiency.

The large-signal response is analyzed at a fixed bias voltage of −3 V, which provides the maximum 3 dB bandwidth. The electrical modulation signals are generated by an arbitrary waveform generator (AWG) with a 92 GSa/s sampling speed and an electrical amplifier and applied to the LN modulator. The electrical input signal to the LN modulator is equalized by a built-in function of the AWG to obtain a flat frequency response. The AC component of the output photocurrent from the PD is separated by a bias tee and amplified by a 50 GHz amplifier. Figure 4(a) shows clear eye openings under data rates ranging from 10 to 20 Gbps with a generated pseudo-random bit sequence ($2^7 - 1$: limited by the AWG's memory) non-return-to-zero signal from the AWG, the result of which is consistent with that of the small-signal measurement. The corresponding bit error rate (BER) versus the average received optical power P_{rec} is shown in Fig. 4(b). We achieved a BER of less than 1×10^{-9} for 20 Gbps at $P_{rec} = -10$ dBm and 10 Gb/s at $P_{rec} = -13$ dBm. The optical sensitivity of the

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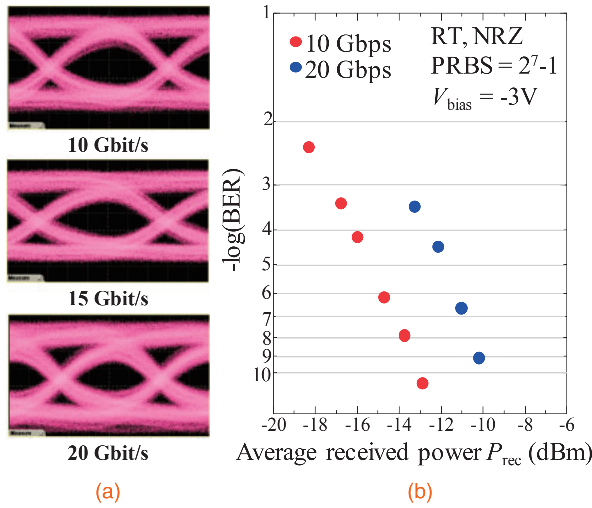

Fig. 4. (a) Eye patterns for different data rates at reverse bias voltage of −3 V. (b) Corresponding BER characteristics.

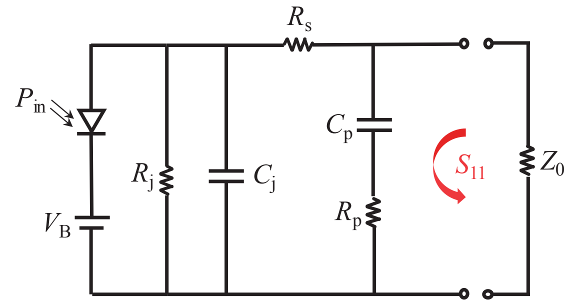

Fig. 5. Equivalent circuit of PD.

Table I. Components extracted from measured S_{11}.

Junction capacitance C_j (fF)	58
Junction resistance R_j (Ω)	6167
Pad capacitance C_p (fF)	11
Pad resistance R_p (Ω)	32
Sheet resistance R_s (Ω)	238

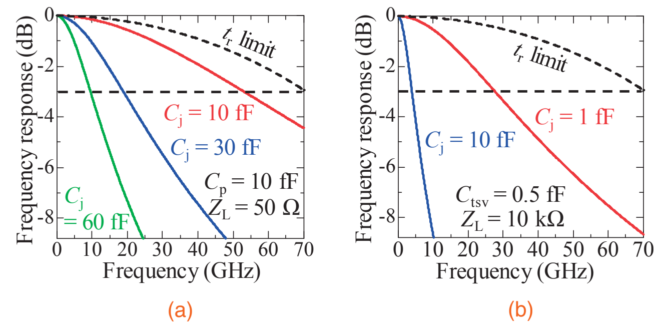

Fig. 6. Frequency response for various C_j values based on (a) current measurement setting and (b) receiverless PD on chip.

photodiode at 10 and 20 Gbps is considered to be limited mainly by an induced error due to changing of the cable connection after calibration. Better configuration of the measurement system might be required to improve the measurement of the optical sensitivity. However, the optical sensitivity is considered sufficient for the lower-power-consumption on-chip optical interconnection considering the laser output of less than 100 µW.

It is necessary to achieve a higher 3 dB bandwidth to fulfill the predicted future demand for on-chip optical interconnections with data rates considerably higher than 20 Gbps.[14] Factors that currently limit the response speed of our PD are investigated by high-speed impedance measurement based on the VNA. It is well known that the net frequency response of a p–i–n PD can be expressed as[15]

$$H(\omega) = H_{RC}(\omega) \cdot H_{transit}(\omega), \tag{1}$$

where $H_{transit}(\omega)$ is the corresponding frequency response related to the interfacial hole trapping or carrier transit time, and $H_{RC}(\omega)$ is the circuit transfer function, that is, the S_{21} response of the equivalent circuit of the PD shown in Fig. 5, where R_j is the junction resistance, C_j is the junction capacitance under a reverse bias condition, R_s is the sheet resistance of the device, Z_0 is the characteristic impedance of 50 Ω, and R_p and C_p are the electrode pad resistance and parasitic capacitance, respectively. All the components mentioned above for estimating the S_{21} response are obtained by measuring the reflection component S_{11} with an input signal from the VNA. The S_{11} and S_{21} responses of the equivalent circuit can be expressed as

$$S_{11} = \frac{Z_p + Z_p Y_j R_s - Z_0(Y_j R_s + Y_j Z_p + 1)}{Z_p + Z_p Y_j R_s + Z_0(Y_j R_s + Y_j Z_p + 1)}, \tag{2}$$

$$S_{21} = \frac{Z_p Z_0}{Z_p Z_0 Y_j + (Z_p + Z_0)(Y_j R_s + 1)}, \tag{3}$$

where $Y_j = 1/R_j + j\omega C_j$, $Z_p = R_p + 1/(j\omega C_p)$. The extracted components based on the fitting curve of the measurement results of both the real part and the imaginary part of S_{11} are listed in Table I. Under the reverse bias condition, the extremely large R_j can be ignored during estimation of S_{21}. The parasitic capacitance of the electrode pads ($C_p = 11$ fF) is determined by the pad area (approximately 5000 µm^2) when the probes are loaded on the device during the experiment. We find that compared to R_p and R_s, the reduction of C_j significantly increases the 3 dB bandwidth under the assumption of unchanged C_p and $Z_0 = 50$ Ω considering the current experimental environment [see Fig. 6(a)]. However, the increase in the 3 dB frequency would be limited by the carrier transit time t_r. Recently, we reported that the introduction of a photonic crystal structure into the in-plane p–i–n PD would provide strongly enhanced lateral optical confinement or the slow-light effect of the GaInAs absorber, resulting in a narrower stripe width for achieving sufficient absorption efficiency.[16,17] A t_r limitation of 70 GHz is calculated by assuming a fully depleted absorption region with a stripe width of 0.3 µm, in which a saturation hole drift velocity of 4.8×10^6 cm/s is assumed to be obtained in the presence of a sufficient electric field.[18] Figure 6(b) shows another estimation of the 3 dB bandwidth of the receiverless PD, which is expected to be introduced in future on-chip optical interconnections. It is predicted that a sufficient output voltage of the PD can be obtained without excessive power consumption of the TIA and PA by replacing them with a load resistance $Z_L = Z_0 = 10$ kΩ.[19,20] Moreover, the electrodes can be removed because the device is actually integrated on an LSI chip, and we assume that through-silicon via with an extremely small parasitic capacitance will

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be used for connecting the PD to the subsequent circuit. According to the calculation result, C_j should be approximately 1 fF, which is far below the value that we have obtained currently, to fulfill the demand for high-speed operation.

To further reduce C_j, we investigate the layer structure of our device, as shown in Fig. 1(b). The calculation result based on the finite element method indicates that the large C_j (approximately 60 fF) is due to the formation of a PN junction between the *p*-InP top cap layer and the *n*-InP side cladding layer in both the absorber and the passive waveguide region (as in the membrane-based laser structure). C_j can be decreased from 0.16 to 0.04 fF/µm in the propagation direction by replacing the *p*-InP cap ($N_A = 3 \times 10^{17}\,cm^{-3}$) with a shallow-doped *n*-InP cap in the absorber region. Moreover, if we use a GaInAsP channel waveguide surrounded by SiO_2 cladding instead of InP claddings,[21] the C_j generated in the passive waveguide region can be further reduced. Therefore, we believe that a device capacitance of approximately 1 fF can be achieved by modifying the device structure.

In conclusion, high-speed operation of a GaInAs membrane-based p–i–n photodiode was reported in this paper. A 3 dB cutoff frequency of 13.3 GHz was achieved at a reverse bias of −3 V. In addition, a BER of less than 1×10^{-9} was achieved at data rates of 20 and 10 Gbps with input powers of −10 and −13 dBm, respectively. The frequency response was considered to be limited by the junction capacitance (approximately 60 fF), which can be reduced significantly by modifying the layer structure. Thus, the 3 dB frequency can be increased, and the demand for a receiverless PD in on-chip optical interconnections can be fulfilled.

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