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BRIEF PAPER *Special Section on Fundamentals and Applications of Advanced Semiconductor Devices*

Type-II HfS_2/MoS_2 Heterojunction Transistors

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SUMMARY We experimentally demonstrate transistor operation in a vertical p^+-MoS_2/n-HfS_2 van der Waals (vdW) heterostructure configuration for the first time. The HfS_2/MoS_2 heterojunction transistor exhibits an ON/OFF ratio of 10^4 and a maximum drain current of 20 nA. These values are comparable with the corresponding reported values for vdW heterojunction TFETs. Moreover, we study the effect of atmospheric exposure on the subthreshold slope (SS) of the HfS_2/MoS_2 transistor. Unpassivated and passivated devices are compared in terms of their SS values and I_{DS}–V_{GS} hysteresis. While the unpassivated HfS_2/MoS_2 heterojunction transistor exhibits a minimum SS value of 2000 mV/dec, the same device passivated with a 20-nm-thick HfO_2 film exhibits a significantly lower SS value of 700 mV/dec. HfO_2 passivation protects the device from contamination caused by atmospheric moisture and oxygen and also reduces the effect of surface traps. We believe that our findings will contribute to the practical realization of HfS_2-based vdW heterojunction TFETs.

key words: *TMDC, MoS_2, HfS_2, tunnel FET, heterojunction*

1. Introduction

Advancements in ultra-large-scale integration (ULSI) have thus far been sustained by the continuous scaling down of Si-based metal–oxide field-effect transistors (MOSFETs) over the last few decades. However, the power consumption of ULSI devices has not seen a corresponding scaling down owing to the fact that the power supply voltage of the transistor cannot be reduced further. The turn-on characteristic of a conventional MOSFET, namely, the subthreshold slope (SS), is governed by the Boltzmann limit wherein thermionic emission across the potential barrier from the source to the channel region is limited by temperature. This Boltzmann limit of SS, which is ~60 mV/dec at room temperature, is the main bottleneck in further scaling down the supply voltage. However, tunneling field-effect transistors (TFETs) are not constrained by the Boltzmann limit by virtue of their band-to-band tunneling (BTBT) carrier injection mechanism, which enables a reduction in the power consumption of ULSI devices using TFETs. Thus, TFETs are a promising candidate for future ultra-low-power electronic devices.

Meanwhile, low-defect density and sharp band edges are crucial to the quality of heterojunctions, which is very important for realizing a high-performance TFET. In this context, transition metal dichalcogenides (TMDs) are promising materials owing to their atomically uniform thickness and sharp band edges. Roy et al. recently published the results of their investigations of MoS_2/WSe_2 [1] and $WSe_2/SnSe_2$ [2] TFETs, and the 2D–2D heterostructure devices fabricated by them exhibited a clear negative differential resistance (NDR), which is direct evidence of BTBT. In addition, Sarkar et al. reported BTBT in devices fabricated using TMD material [3], wherein a p^+-Ge/MoS_2 heterostructure (3D–2D) exhibited the lowest SS value of 3.9 mV/dec over several decades of drain current.

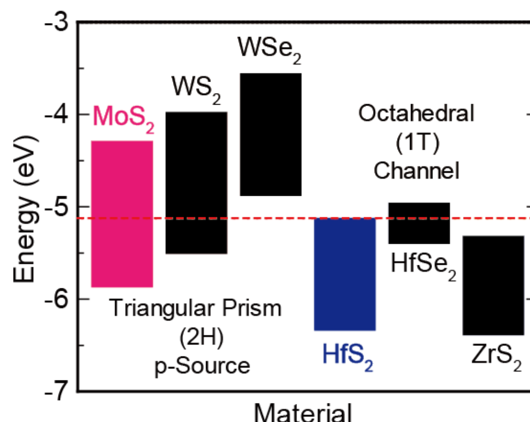

Fig. 1 Band alignment in monolayer transition metal dichalcogenide (TMD) semiconductors (MoS_2, WS_2, WSe_2, HfS_2, $HfSe_2$, and ZrS_2) [4]. The dotted red line indicates the conduction band level of HfS_2; the vacuum level is at 0 eV.

In this paper, we report the fabrication process and results for transistors with a vertical HfS_2/MoS_2 van der Waals (vdW) heterostructure. Among the TMD materials shown in Fig. 1 [4], HfS_2 has high electron affinity, which results in a large band discontinuity when heterojunctions are formed with other TMD materials such as MoS_2. This is expected to facilitate TFET operation resulting in a high drain current.

2. Fabrication Process of HfS_2/MoS_2 Heterojunction

Figure 2 shows the schematic cross-section of the fabricated device. As the (back) gate insulator, 25 nm of Al_2O_3 film was deposited on a highly doped n^{++} Si substrate by plasma ALD. Thin HfS_2 flakes were mechanically exfoliated on the substrate by use of the Scotch-tape method (Fig. 3 (a)).

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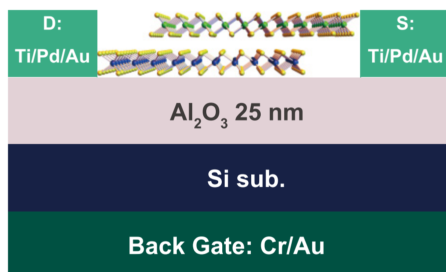

Fig. 2 Schematic cross-section of back-gated transistor with vertical HfS_2/MoS_2 van der Waals (vdW) heterostructure on 25-nm-thick Al_2O_3/n^{++}-Si substrate.

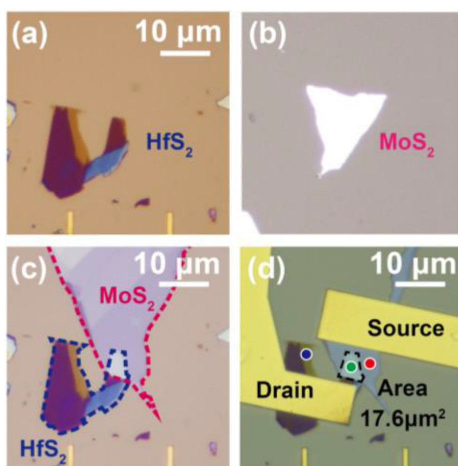

Fig. 3 Optical images of (a) transferred HfS_2 flake on Al_2O_3, (b) transferred MoS_2 flake on polydimethylsiloxane (PDMS), (c) vertical HfS_2/MoS_2 heterostructure, and (d) device with Ti/Pd/Au source and drain contacts.

Similarly, MoS_2 flakes were transferred onto polydimethylsiloxane (PDMS) (Fig. 3 (b)). To form the HfS_2/MoS_2 heterojunction, a suitable MoS_2 flake on PDMS was transferred onto HfS_2 (Fig. 3 (c)) by means of a micromanipulator alignment system [5], creating 17.6 μm^2 of heterojunction area. Subsequently, source and drain electrodes (Ti/Pd/Au: 20 nm/20 nm/80 nm) and a back-gate electrode (Cr/Au: 20 nm/100 nm) were formed by electron beam evaporation (Fig. 3 (d)). Finally, to improve the device characteristics, vacuum annealing was performed at 250°C for 1 h [6]. Nb-doped p-type MoS_2 (doping concentration of $\sim 10^{19}$ cm^{-3}) with a purity of 99.99% was used as the source layer.

3. Device Results of HfS_2/MoS_2 Heterojunction Transistor

3.1 Confirmation of p-Type Behavior of MoS_2

We first confirmed the p-type behavior of MoS_2 at various back-gate voltages since our proposed device has a global back-gate structure to modulate the n-HfS_2 channel, and this is expected to affect the p-MoS_2 source layer. The I–V characteristics of the p-MoS_2 MOSFET shown in Fig. 4 illustrate that as the back-gate voltage (V_{BG}) is increased to positive values, the slope of the current characteristic gradually reduces. This is due to the fact that the resistivity of the MoS_2 channel increases as holes are expelled. This result confirms that the MoS_2 flake used in our device is a p-type semiconductor even when a strong positive bias is applied.

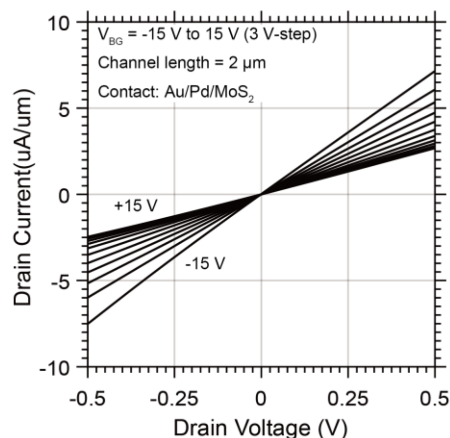

Fig. 4 I–V characteristics of Nb-doped MoS_2 metal–oxide field-effect transistor (MOSFET), indicating p-type behavior.

3.2 TEM and Raman Measurements of HfS_2 and MoS_2 Flakes

The band alignment of the heterojunction is a crucial parameter for archiving a high-performance TFET, as mentioned previously. In addition, the layer thickness of TMD materials forms another key parameter in 2D heterojunctions due to the fact that the band gap of the TMD materials varies depending on its layer thickness. Thus, before examining the electrical characteristics of HfS_2/MoS_2 heterojunction transistor, we performed transmission electron microscopy (TEM) and Raman measurements in order to evaluate the layer thickness of HfS_2 and MoS_2 flakes used in our device.

The layer thicknesses of the HfS_2 and MoS_2 flakes were confirmed by means of TEM. The TEM images clearly show 10-nm-thick HfS_2 (Figs. 5 and 6) and 5-nm-thick MoS_2 flakes (Fig. 5). Furthermore, from Fig. 6, the thickness of a monolayer of HfS_2 can be estimated as 0.58 nm, which is found to be in good agreement with the theoretical value (0.59 nm) [6]. It is assumed that flakes with bulk-like characteristics are stacked together. The Raman spectra of the fabricated device excited by a 532-nm laser line are shown in Fig. 7. The Raman spectra were obtained at positions corresponding to the red, green, and blue marks in Fig. 3 (d) for MoS_2, HfS_2, and the HfS_2/MoS_2 heterostructure, respectively. The characteristic Raman peaks of both HfS_2 (A_{1g}: 337 cm^{-1}) and MoS_2 (E_{2g}: 384 cm^{-1}, A_{1g}: 407 cm^{-1}) were observed at the heterojunction area. The peak position of MoS_2 A_{1g} (~ 407 cm^{-1}) spectra observed in the MoS_2 flake (red mark in Fig. 3 (d)) indicates that MoS_2 flakes possess bulk properties [7], and this corresponds with

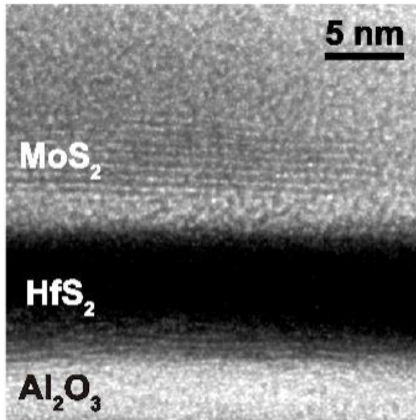

Fig. 5 Cross-sectional transmission electron microscopy (TEM) image of HfS_2/MoS_2 van der Waals (vdW) heterostructure, showing 10-nm-thick HfS_2 and 5-nm-thick MoS_2 in field of view.

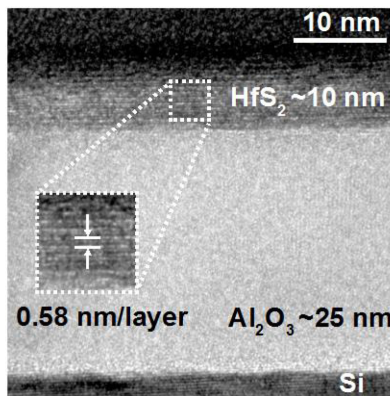

Fig. 6 Cross-sectional transmission electron microscopy (TEM) image of HfS_2 flake on 25 nm of Al_2O_3. A HFS_2 monolayer of 0.58 nm was observed for the first time experimentally.

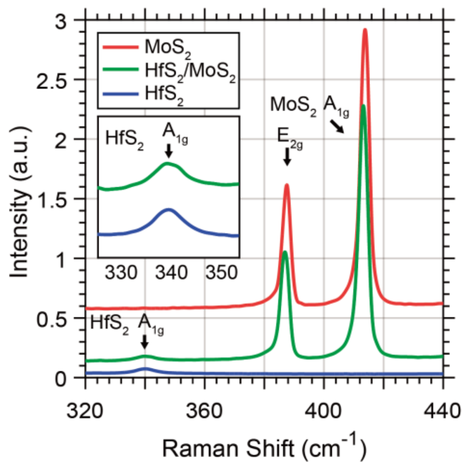

Fig. 7 Raman spectra of bulk-like HfS_2 flake (blue curve), MoS_2 (red curve), and HfS_2/MoS_2 heterostructure (green curve). Inset shows the A_{1g} peak of HfS_2 on the flake and at the HfS_2/MoS_2 heterojunction.

the thickness of the MoS_2 flake obtained from TEM images.

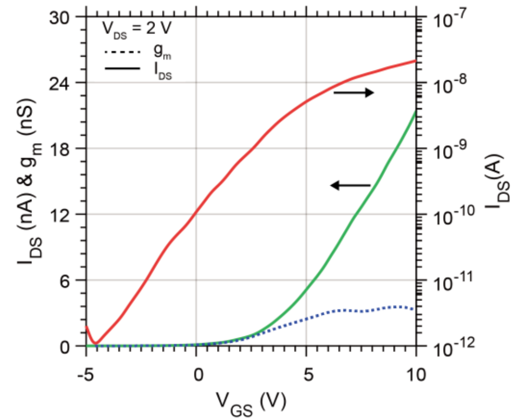

Fig. 8 Transfer characteristics of HfS_2/MoS_2 heterojunction transistor at V_{DS} = 2 V. Red, green, and blue lines indicate I_{DS} on a logarithmic scale, I_{DS} on a linear scale, and transconductance, respectively.

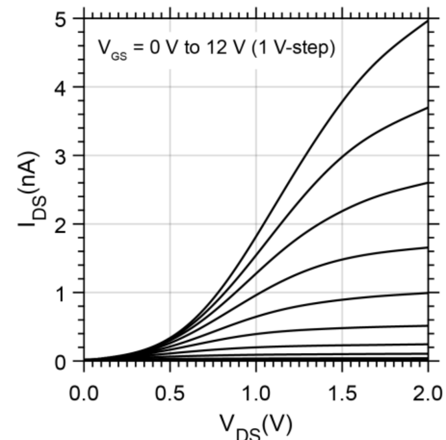

Fig. 9 Output characteristics of HfS_2/MoS_2 heterojunction transistor as function of V_{GS} (back-gate).

3.3 Electrical Characteristics of HfS_2/MoS_2 Heterojunction Transistor

The electrical characteristics of our back-gate HfS_2/MoS_2 transistor are shown in Figs. 8 and 9. Figure 8 depicts four decades of the ON/OFF ratio (red line) and 20 nA of the maximum drain current (green line) at V_{GS} = 10.0 V and V_{DS} = 2.0 V. The maximum drain current is comparable with that of other TFETs with vdW heterojunctions [1], [2]. Moreover, we performed two-terminal measurements using the source and drain terminals (V_G = 0 V) to verify the rectifying behavior of the heterojunction. This is shown in Fig. 10, which reflects the formation of the p–n junction with vdW heterointerfaces.

4. HfO_2-Passivation of HfS_2/MoS_2 Heterojunction Transistor

It is known that HfS_2 is severely affected by atmospheric contaminants such as oxygen and moisture, which results in

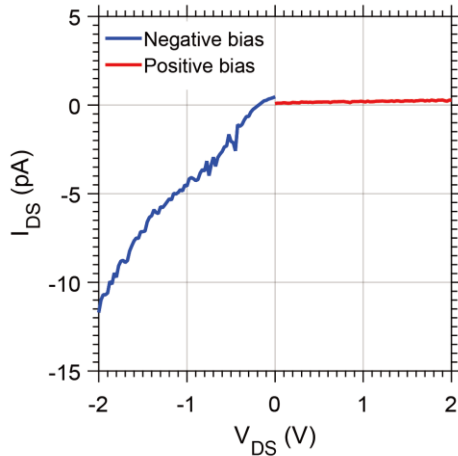

Fig. 10 Two-terminal characteristics (for $V_G = 0$ V) of HfS_2/MoS_2 heterojunction transistor. The drain terminal (HfS_2 side) was defined as positive in this graph. The slight difference in the current at 0 V is due to the influence of the transient response at the start of each measurement.

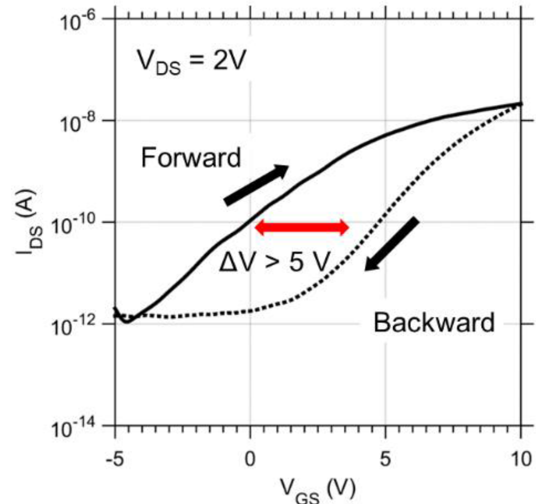

Fig. 11 I_{DS}–V_{GS} characteristic of unpassivated device measured in air. This result corresponds to the same device whose characteristics are shown in Fig. 8. $\Delta V_{hysteresis} > 5$ V.

poor device performance [8], [9]. Therefore, an appropriate passivation layer such as HfO_2 is considered to be essential for HfS_2 MOSFETs [10] and for HfS_2/MoS_2 heterojunction transistors as well. To study the effect of the HfO_2 passivation layer, we fabricated another HfS_2/MoS_2 heterojunction transistor prototype. The same fabrication steps were followed before final deposition of a 20-nm-thick HfO_2 film on top of the device surface. This passivation layer covered both the heterojunction and the access regions (the region from S/D contacts to the heterojunction) of the device. The heterojunction area was deduced to be 38.23 μm^2 in this device, and the TEM images confirmed the thicknesses of HfS_2 and MoS_2 to be 10 nm and 90 nm, respectively. Figures 11 and 12 depict the I_{DS}–V_{GS} characteristics of the unpassivated and passivated devices, respectively. In the unpassivated device (Fig. 11), the estimated average value of SS was 2000 mV/dec and the hysteresis was $\Delta V = 5$ V. A clear reduction in hysteresis was observed in the passivated device (Fig. 12), which exhibited a $\Delta V_{hysteresis}$ of 0.5 V. Furthermore, the minimum SS value of 700 mV/dec was observed for the passivated device, and this value is one-third of that observed in the unpassivated device. This reduction in hysteresis and lower SS value indicate that the HfO_2 passivation layer effectively reduces the surface trap density at the heterojunction.

From Fig. 12, we observe that hysteresis is drastically reduced by HfO_2 capping; however, a small hysteresis is still discernible. To improve the device performance further, it is important to understand the origin of hysteresis, which is in turn governed by the trap location. The two possible trap locations are: 1) access regions (HfO_2/MoS_2, HfO_2/HfS_2) and the area above the heterojunction (HfO_2/heterojunction), and 2) within the heterojunction (HfS_2/MoS_2) interface. To estimate the magnitude and to identify the cause of the hysteresis, the passivated device (shown in Fig. 12) was subjected to I–V characteristic measurement in a vacuum chamber (10^{-6} Torr). The resulting I–V curve in Fig. 13 shows

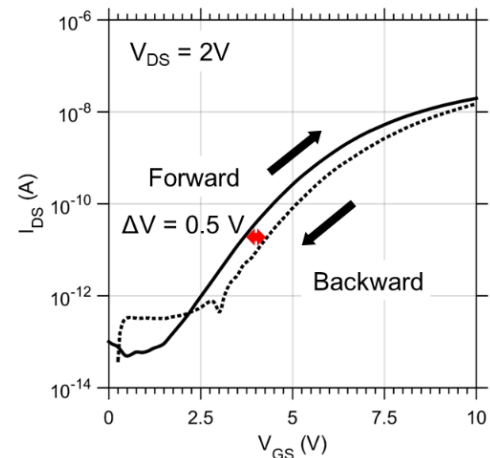

Fig. 12 I_{DS}–V_{GS} characteristic of HfO_2-passivated device measured in air. $\Delta V_{hysteresis} = 0.5$ V.

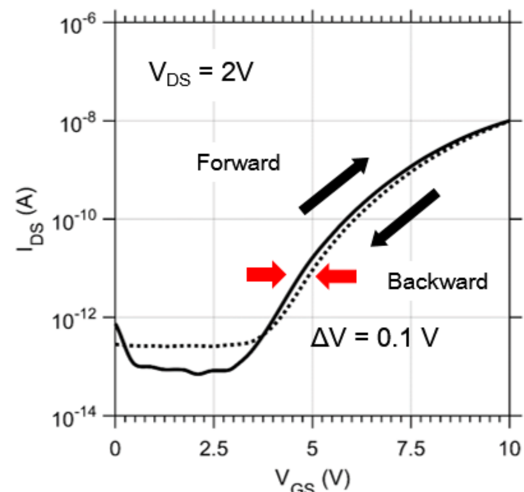

Fig. 13 I_{DS}–V_{GS} characteristic of passivated device measured in vacuum (10^{-6} Torr).

that $\Delta V_{hysteresis}$ is further reduced to approximately 0.1 V. Considering that this is a surface phenomenon, we believe that traps and defects present in the access regions and above the heterojunction (case 1) are stabilized or desorbed through the thin HfO_2 (20 nm) film under high vacuum. Since MoS_2 (90 nm) is considerably thicker than HfO_2, the process of outgassing or gettering of contaminants from the heterojunction, thought to be the origin of traps and/or defects, becomes more difficult.

5. Conclusion

We have demonstrated for the first time a HfS_2/MoS_2 heterojunction transistor with an ON/OFF ratio of 10^4 and I_{DS} of 20 nA. In addition, the formation of a p–n junction with vdW heterointerfaces was confirmed. A clear reduction in hysteresis and improvement in the SS value were evidenced in the HfO_2-passivated HfS_2/MoS_2 heterojunction structure, thereby highlighting the role of contaminants acting as surface traps in the ambient environment. Although we have successfully improved the performance of the HfS_2/MoS_2 heterojunction transistor, no direct evidence of BTBT was observed. Our future works will therefore focus on obtaining direct evidence of BTBT, such as NDR or an SS of < 60 mV/dec.

Acknowledgments

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