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# Si-Photonics-Based Layer-to-Layer Coupler Toward 3D Optical Interconnection*

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**SUMMARY** To realize three-dimensional (3D) optical interconnection on large-scale integration (LSI) circuits, layer-to-layer couplers based on Si-photonics platform were reviewed. In terms of optical cross talk, more than 1 $\mu$m layer distance is required for 3D interconnection. To meet this requirement for the layer-to-layer optical coupler, we proposed two types of couplers: a pair of grating couplers with metal mirrors for multi-layer distance coupling and taper-type directional couplers for neighboring layer distance coupling. Both structures produced a high coupling efficiency with relatively compact (~100 $\mu$m) device sizes with a complementary metal oxide semiconductor (CMOS) compatible fabrication process.

***key words:*** *Si photonics, 3D optical interconnection, layer-to-layer coupler, grating*

## 1. Introduction

Recent progress in computing technologies has gradually changed people's daily lives, such as Internet of Things (IoT) and artificial intelligence (AI). These computing technologies rely on high-end large-scale computing systems in super computers or data centers. To enhance computing speed, optical interconnections have recently become important to ensure large enough I/O bandwidths, essential for parallel computing. Therefore, modern data centers have installed optical interconnections between centers, racks, and boards. Furthermore, in state-of-the-art super computers, attempts have been made to install the optical interconnection even inside the boards. Ultimately, optical interconnection on electrical large-scale integration (LSI) circuits should be the target to enhance computing speed. To realize such on-chip interconnections, we proposed semiconductor membrane InP-based photonic integrated circuits (PICs) and demonstrated low threshold and high efficiency lasers on an Si substrate [1]–[4].

We also proposed to integrate an amorphous-silicon (a-Si) layer on conventional crystalline-silicon (c-Si) to realize three-dimensional (3D) stacks [5]. In fact, recent electrical LSIs have multi (~10) electrical wiring layers on a complementary metal oxide semiconductor (CMOS) layer. Therefore, we believed it was a natural progression to develop 3D stacks, even for PICs. Figure 1 shows the image of a 3D opto-electronic integrated-circuit (3D-OEIC) drawn in our internal proposal when we started the project 10 years ago. Optical transaction, optical I/O, and light source layers (in the InP-based membrane PICs) were placed on the electrical transaction layers, including the CMOS transistors. Except for the top light source layer, all other layers consisted of Si or Si-based materials. If this type of OEIC chip could be realized, the signal transaction speed by one single chip, as well as parallel computing, would be significantly enhanced, since there would be essentially no limitation in the wiring bandwidth.

Moreover, this 3D stack technology can be used to reduce the footprint of photonic modules, especially when multiplexing transmission systems, such as wavelength division multiplexing (WDM), are used. Usually, the sizes of multiplexers or demultiplexers are large. If these large components can be stacked vertically the total size of the circuits can be reduced [6].

To realize these 3D stacks of photonic layers on CMOS circuits, process compatibility is very important. One way to ensure this compatibility is by using bonding methods after a separate fabrication process for each stacked wafer. Another simple way is by direct stacks using deposition methods. However, there is the limitation of process temperature. Since the thermal tolerance of the CMOS layer is usually less than 400°C, we cannot deposit c-Si, which requires a much higher temperature, on the CMOS layer. In contrast, the deposition temperature of a-Si is ~300°C. Therefore, multiple stacking of photonic layers with an a-Si core is well suited for 3D optical interconnection. In Sect. 2, the

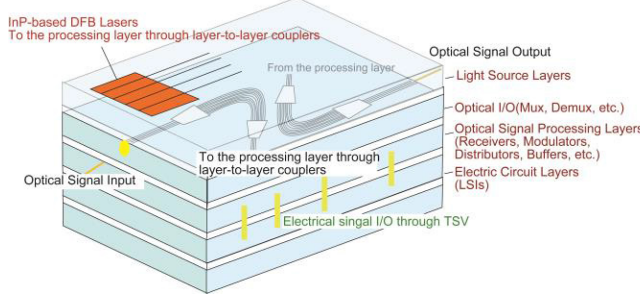


**Fig. 1** Image of 3D OEICs.

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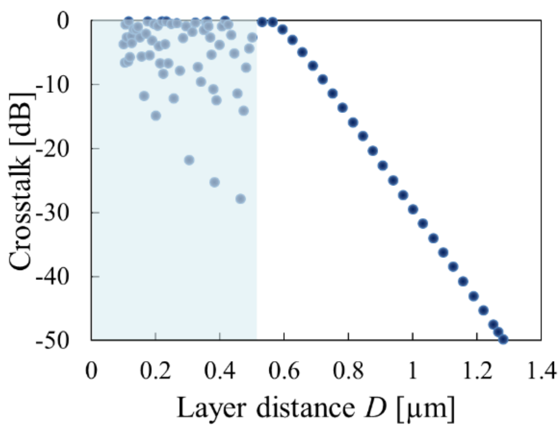



**Fig. 2** Optical crosstalk between two Si core layers after propagation in 100 $\mu$m length waveguides as a function of layer distance [8].

basic characteristics of such a-Si stacking is described.

Coupling the signal between layers is also a critical issue to be solved for realizing 3D optical interconnection. If the interlayer thickness between the layers is relatively thin (< few hundred nm), a simple directional coupler type device with linear taper structure is sufficient [7]. However, such small interlayer thickness produces unwanted signal crosstalk between layers. Our calculation shows the interlayer thickness of cladding material (usually $SiO_2$) between layers should be more than 1 $\mu$m to suppress the crosstalk to less than −30 dB as shown in Fig. 2 [8] To achieve signal coupling with a relatively thick interlayer thickness, several proposals were demonstrated [9], [10]. We proposed two types of couplers. The first is a grating-type coupler, that achieved several-$\mu$m distance coupling; e.g. from the 1st to the 3rd layer coupling. The other is a directional coupler-type structure with double or curved-shape tapers for neighboring layer coupling. The characteristics of these couplers are reviewed in Sects. 3 and 4.

## 2. Basic Characteristics of a-Si:H Layer for 3D Stack

As mentioned in Sect. 1, a-Si is a core material for 3D stacks in optical interconnections. To reduce the material loss of the a-Si, we used a hydrogenated a-Si (a-Si:H) structure using plasma enhanced chemical vapor deposition (PECVD). The material gases were $SiH_4$ and Ar. The RF (13.56 MHz) power of the plasma was 100 W and the chamber pressure was 30 Pa. The chamber temperature was set to 300°C. For the 3D optical interconnection, the fabrication process was as follows: First, $SiO_2$ was deposited by PECVD for the bottom cladding layer. Then, the a-Si:H layer with a thickness of 220 nm was deposited, under the aforementioned conditions. The waveguide patterns were exposed by electron-beam lithography, followed by Si etching using $CF_4$ inductively-coupled-plasma reactive-ion-etching (ICP-RIE). Again, $SiO_2$ was deposited as a cladding layer between the core layers. However, after the deposition, the surface did not have a flat surface. Therefore, chemical mechanical polishing (CMP) was carried out. After CMP, the surface roughness (root-mean-square: RMS) was ~0.31–0.39 nm. Then, another a-Si layer was deposited and the process continued until the desired number of layers was obtained. By introducing CMP process, the film quality of a-Si might be concerned since the film quality of a-Si is sensitive to the film condition of the underneath layer. To check this, we carried out ellipsometry measurements. Figures 3(b) and 3(c) show the refractive index and absorption spectra of a-Si. The three lines in the figures correspond to the different samples, a-Si on the $SiO_2$/Si substrate, a-Si on the $SiO_2$/SOI substrate, and a-Si on the $SiO_2$/a-Si/$SiO_2$/Si substrate as shown in Fig. 3(a). For the latter two samples, CMP was carried out before the a-Si:H deposition. No difference was observed in the material properties even after the CMP process. The material absorption at a wavelength of 1.55 $\mu$m was negligible. Using this process, the transmission loss of the Si-waveguides as a function of layer number was measured. The size of the Si-waveguide cores was 500

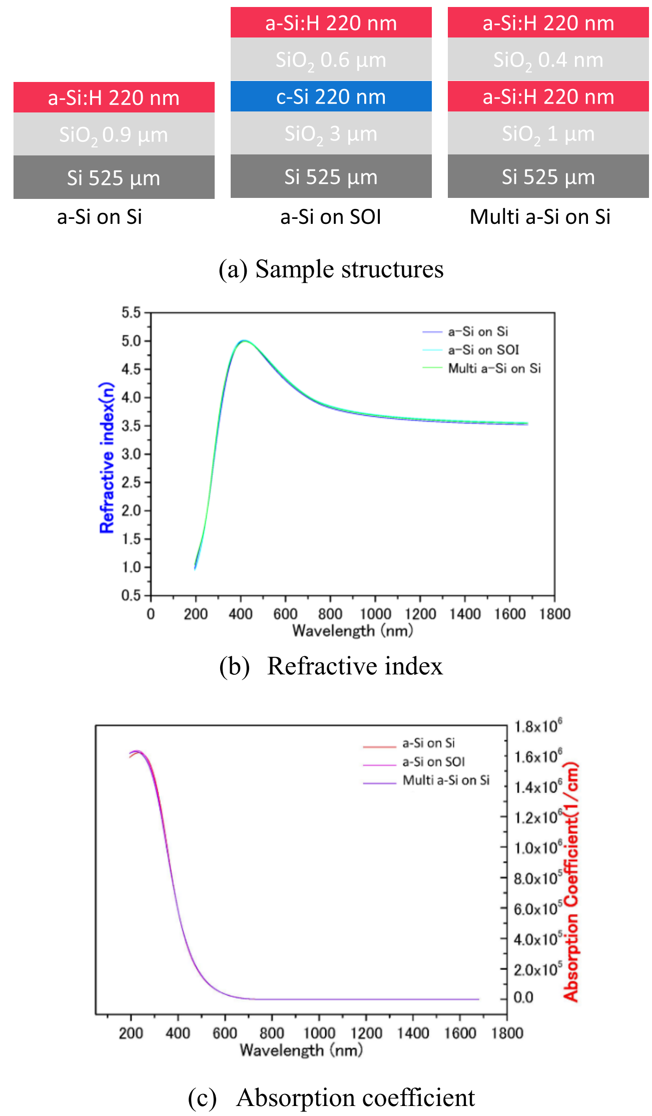


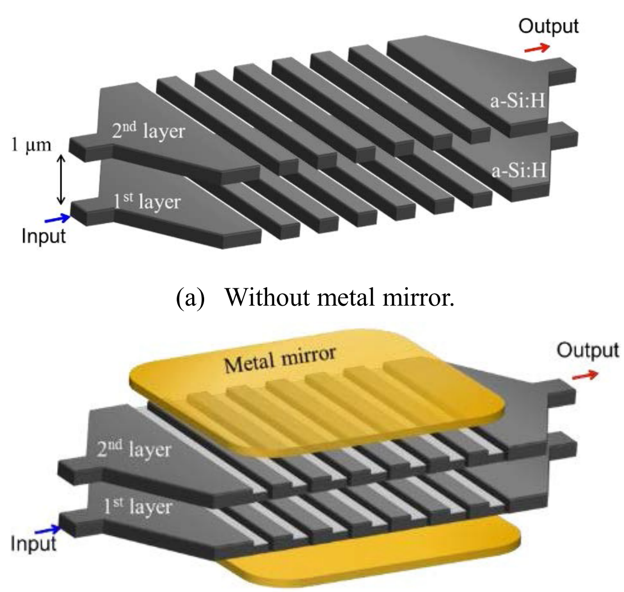

**Fig. 3** Optical properties of a-Si:H.

nm x 220 nm and the interlayer thickness between the a-Si cores was 1 $\mu$m. In this experiment, c-Si was used for the first layer and a-Si:H was used for second and third layers. The observed transmission losses of the first, second, and third layers were 1.2, 3.8, and 3.7 dB/cm, respectively. Although some degradation was observed, a relatively low transmission loss was achieved for stacks up to 3-layers.

## 3. Grating Coupler with Metal Mirrors

In this section, grating-type layer-to-layer couplers are reviewed. As mentioned in Sect. 1, the layer-to-layer distance should be at least 1 $\mu$m. Changing the light propagation direction to upward/downward using a grating is an effective way to couple light over large distances. By introducing a pair of grating couplers, the light signal can move from one layer to another. Figures 4(a) and 4(b) show the images of the grating-type layer-to-layer couplers. Two kinds of couplers were demonstrated. One had a pair of gratings (Fig. 4(a)) [8], [11]. The other had a pair of gratings with metal mirrors at the bottom and top of the grating couplers (Fig. 4(b)) [12], [13].

The fabrication process was essentially the same as that explained in Sect. 2. For the case with metal mirrors, the metallization process by electron-beam evaporation was also performed. In our experiment, gold was used for the mirror material due to equipment limitations. However, Aluminum is also suitable (almost same coupling performance can be achievable according to our calculation) and is commonly used in CMOS processes. To control the $SiO_2$ thickness by CMP, *ex-situ* thickness monitor measurements were used. Figure 5 shows a scanning electron microscope (SEM) image of the coupler with metal mirrors. The thickness targets for the mirror-to-Si core and core-to-core were 800 and 1000 nm, respectively. The thickness error was as small as 10 nm. Figure 6 shows the transmittance spectra of the grating coupler with and without metal mirrors. The grating structure consisted of the period of 640 nm with 50% duty cycle, the repetition of 20 times, and the waveguide width of 5 $\mu$m. The TE-polarized light was input from the 1st layer and the output light from the 2nd layer was observed. It clearly showed a higher coupling efficiency of 83% for the device with metal mirrors, compared with an efficiency of 22% for the device without the metal mirror. For the one with metal mirrors, the output light power from the 1st layer was under the measurement limit. Without the metal mirror, the light from the grating radiated equally both upward and downward, and only half of the radiated power was captured. By introducing the metal mirrors, the downward radiated power was reflected. If the thickness between the mirror and the core coincided for the in-phase condition, the amount of upward optical power was enhanced. Figure 7 shows the intensity profiles of the upward radiated light of the grating for different thicknesses of the mirror and core $D_M$. With a thickness of 800 nm, there was a threefold increase in the intensity compared with that without mirror.




(a) Without metal mirror.

(b) With metal mirrors.

**Fig. 4** Grating-type layer-to-layer couplers [8], [11]–[13].

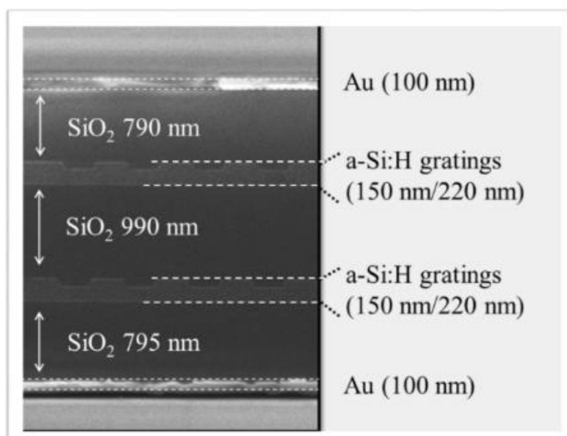



**Fig. 5** SEM image of the fabricated coupler [12].

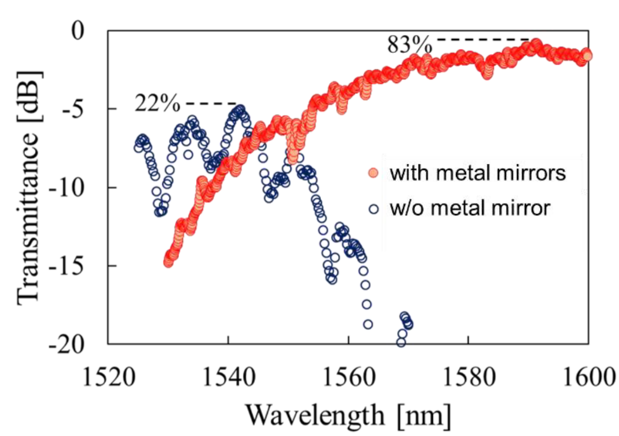



**Fig. 6** Transmittance spectra of the fabricated coupler. The red and blue points are the devices with and without metal mirrors, respectively [12].

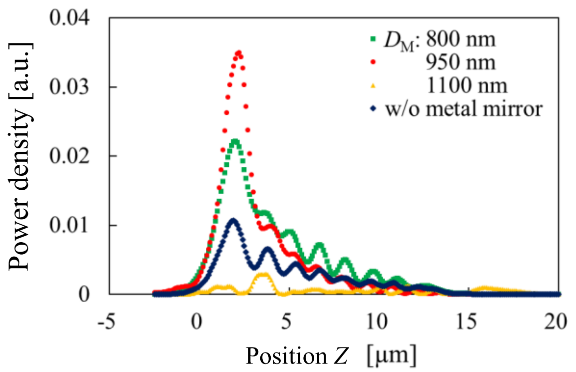



**Fig. 7** Calculated intensity profiles of the upward radiated light from the grating. $z$ is the position along the waveguide light propagation direction. The origin of $z$ is the position of the first grating trench.

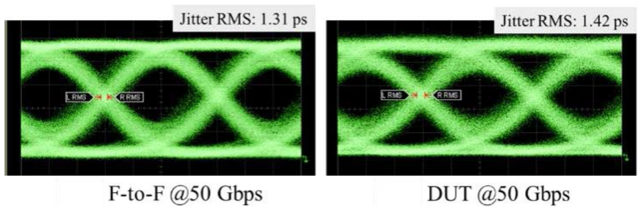



**Fig. 8** Eye diagram under 50 Gbps data transmission through the fabricated grating coupler with metal mirrors [12].

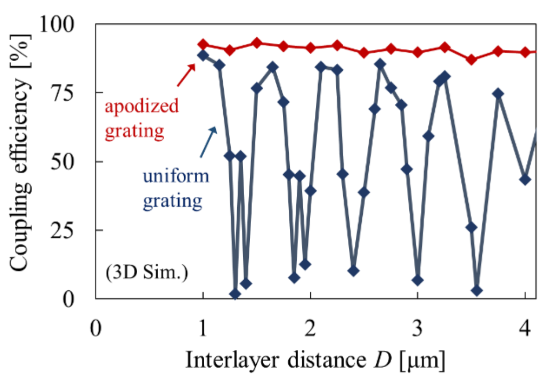



**Fig. 9** Change in transmission distance with the coupling efficiency for uniform (blue) and apodized (red) gratings [14].

For a thickness of 1100 nm, the intensity decreased due to the out-of-phase condition. This parameter was most sensitive for coupling efficiency. Other parameters such as the alignment between the couplers had wider tolerance. Detailed information about design and tolerance is in our previous publication Ref. [13].

Figure 8 shows the eye diagram under 50 Gbps data transmission through the grating coupler with metal mirrors. We could not observe any degradation after the transmission. Although this grating coupler pair with uniform grating duty ratio achieved a high coupling efficiency for a given thickness, it was strongly dependent on the transmission distance, as shown in Fig. 9. This is because the profile of the radiated power was not symmetric and the profiles of the

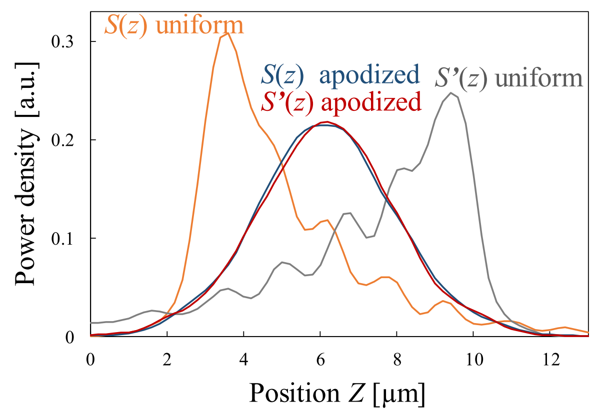



**Fig. 10** Calculated intensity profiles of radiated light from $S(z)$ and $S'(z)$ of the bottom and top gratings, respectively. $z$ is the position along the waveguide light propagation direction.

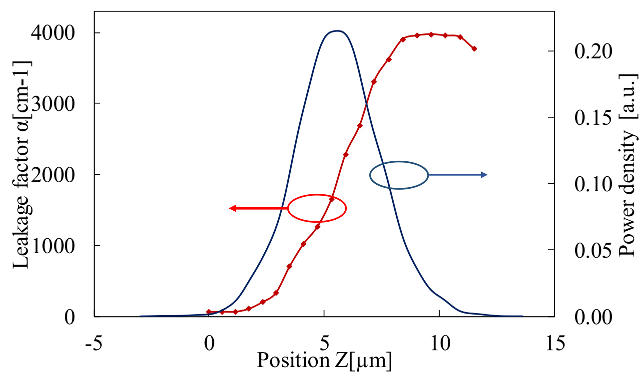



**Fig. 11** Leakage factor at each position of the grating (red) and the calculated intensity profile from the designed apodized grating (blue). $z$ is the position along the waveguide light propagation direction.

bottom and top gratings were not equal, as shown in Fig. 10 (the lines of $S(z)$ and $S'(z)$ uniform). This can be solved by introducing apodization of the grating duty to control the leakage factor at each position of the grating. By adjusting the duty ratio at each position as shown in Fig. 11, the radiation intensity profile was tuned. After adjusting the profile, the radiation profiles of the bottom and top gratings were well matched as shown in Fig. 10 (the lines of $S(z)$ and $S'(z)$ apodized), resulting in a coupling efficiency with almost no dependence on the transmission distance [14].

These results indicated several-$\mu$m transmission was possible using the apodized structure. Therefore, direct layer-to-layer coupling with jumping several layers can be possible.

## 4. Directional Coupler with Complex Taper Structure

If the signals transmit only to neighboring layers, a much simpler structure can be used; a directional coupler structure with tapers. The layer-to-layer directional coupler with linear tapers were demonstrated with an interlayer thickness of 200 nm [7]. However, as mentioned before, at least 1 $\mu$m was needed to reduce unwanted crosstalk. By introduc-

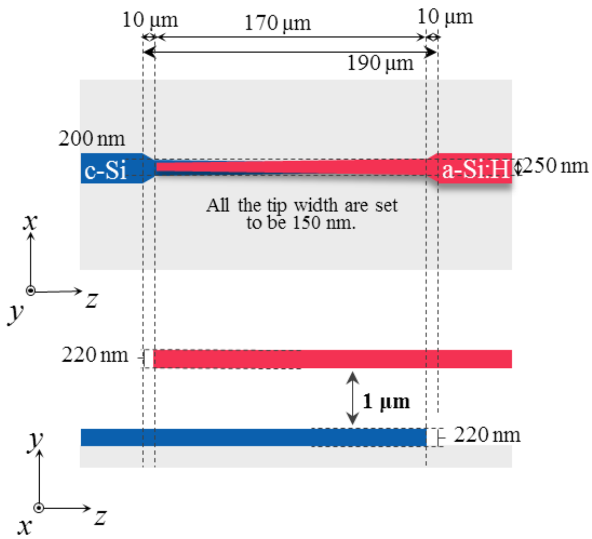



**Fig. 12** Schematic structure of a directional coupler with double taper.

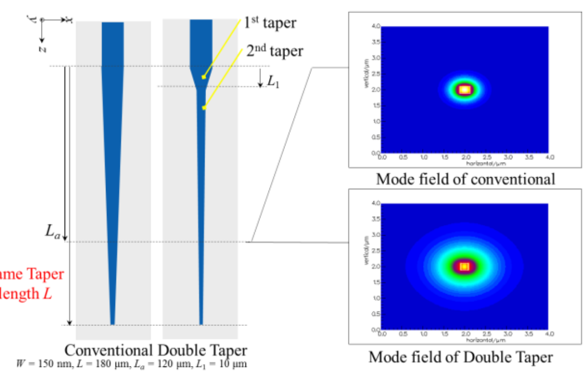



**Fig. 13** Optical mode field at the same position (120 $\mu$m from the start point of the tapers) for conventional and double taper structures under same the taper length design.

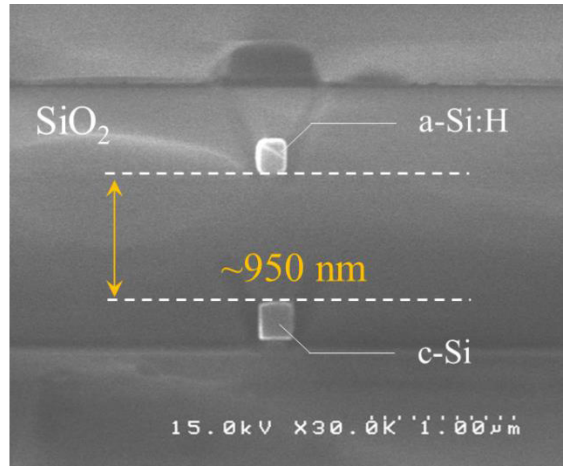



**Fig. 14** SEM image of the center of the fabricated couplers with a double taper structure.

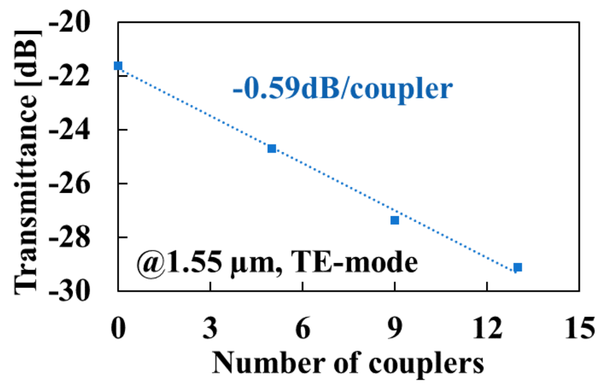



**Fig. 15** Transmittance through the fabricated Si waveguides and couplers as a function of number of couplers. The Interlayer distance was ~1 $\mu$m.

ing the linear taper structure for such a thickness, the length of the coupler becomes cm-order. In contrast, a double taper structure was proposed to reduce the length, as shown in Fig. 12 [15]. The taper was divided into two sections. One had a steep slope angle and the width of the waveguide was varied from 500 to 200 nm for c-Si and 250 nm for a-Si:H. In this section, the size of the optical mode was rapidly widened while maintaining an adiabatic coupling condition. The other section had a moderate slope angle. Optical coupling occurred mainly in this section. Figure 13 shows the comparison of the optical mode field size at the same position for conventional linear and double taper structures. A larger field size was clearly observed for the double taper structure. For a total length of 190 $\mu$m, a coupling efficiency of 96% was achieved in the theoretical calculation for the TE-mode light. Figure 14 shows a SEM image of the fabricated double taper structure. The fabrication process was the same as the aforementioned description. Although a combination of c-Si and a-Si:H was used in this experiment, other combinations are possible, such as a-Si:H/a-Si:H and c-Si/InP membrane. The coupling efficiency was estimated using measurements of the transmittance of couplers by changing the number of couplers that light experiences. The TE-mode light was input to waveguides with different numbers of the couplers. The coupling efficiency was derived from the slope of the fitting curve of transmittance as a function of the number of couplers. A coupling efficiency of 0.59 dB/coupler (87%) was obtained from the results shown in Fig. 15. Please note the value contained the insertion loss of the coupler itself. This value was slightly lower than that of the theoretical calculation and the reason for this is the topic of future research. A similar structure could be also designed for the TM-mode. The alignment tolerance was much wider than the accuracy of conventional stepper (< 50 nm) used in CMOS fabrication process. More detailed information about design and tolerance is in our previous publication Ref. [15].

For a further reduction of the coupler size, a directional coupler with curved taper structure was proposed [16]. Figure 16 shows the structure of the proposed coupler. The shape of the tapers was determined by the function $\sqrt{z}$,

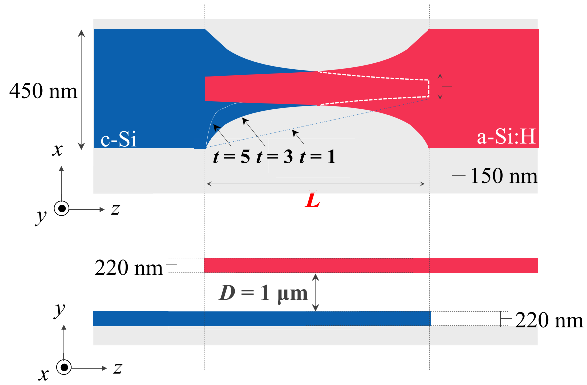



**Fig. 16** Schematic structure of a directional coupler with curved tapers [16].

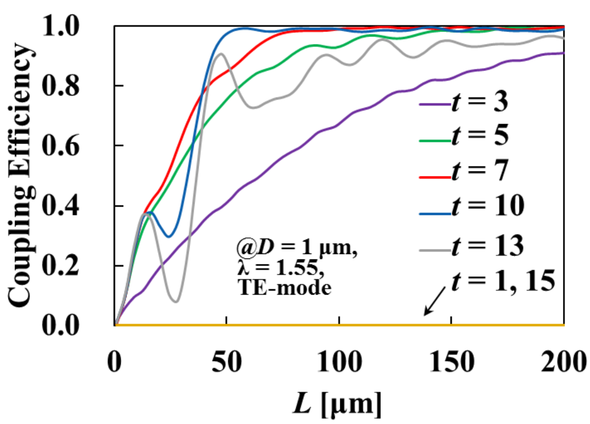



**Fig. 17** Coupling efficiency for various $t$ values as a function of total taper length [16].

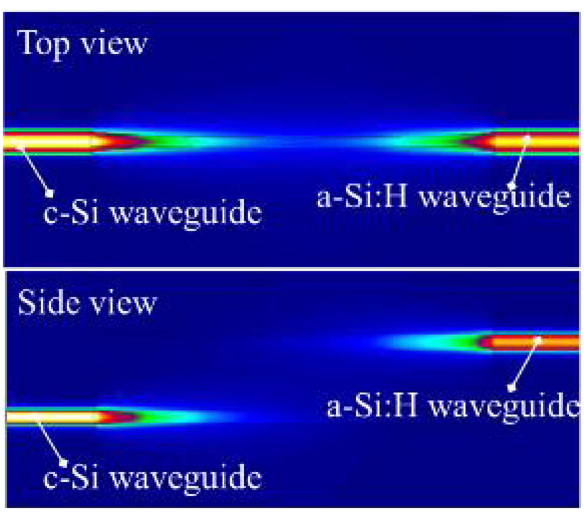



**Fig. 18** Intensity profile of the coupler with a taper shape of $t$ = 7.

where $z$ is the position along waveguide propagation direction and $t$ is the order of the root. If $t$ equals 1, the shape is linear. Figure 17 shows the calculated coupling efficiency for various values of $t$ as a function of total taper length $L$, with an interlayer thickness $D$ of 1 $\mu$m. For $t$ values of 7 or 10, a high coupling efficiency (98%) was achieved with taper lengths of 90 and 60 $\mu$m, respectively. Please note the fabrication tolerance was low for the case of $t$ = 10. To achieve > 80% coupling, less than 40 and 20 nm accuracies were needed for the widths of the waveguide, for the cases of $t$ = 7 and $t$ = 10, respectively. Figure 18 shows the intensity profile along the propagation direction for the case of $t$ = 7. A smooth transition was observed without scattering or reflection. By introducing this structure, a 1/100 size reduction was possible compared with the conventional linear taper structure for a 1-$\mu$m interlayer thickness.

## 5. Conclusion

Structure and characteristics of several types of layer-to-layer couplers were reviewed for 3D optical interconnections on a Si-platform. A CMOS compatible fabrication process with low loss a-Si:H and chemical mechanical polishing were used to produce the photonic layer stack with a relatively low transmission loss. For layer-to-layer couplers, a pair of grating couplers with metal mirrors for multi-layer jumping coupling and a directional coupler with taper structure for the neighboring layer coupling were proposed. A coupling efficiency of > 80% for the fabricated devices with interlayer thicknesses of 1 $\mu$m was demonstrated. We believe this technology shows great potential for the future of 3D high density optical interconnections.

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