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REGULAR PAPER

Highly efficient double-taper-type coupler between III–V/silicon-on-insulator hybrid device and silicon waveguide

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An optical mode converter between hybrid device and Si waveguide is the key component for efficient and stable operation of III–V/silicon-on-insulator (SOI) hybrid photonic integrated circuits (PICs). In this study, we introduced a double taper structure into such a mode converter and investigated the coupling efficiency dependence on their structural parameters. By using N_2 plasma activated bonding technology, III–V/SOI double-taper-type mode couplers with various taper-tip-widths and taper lengths were fabricated, and their coupling efficiencies were evaluated. As the result, a coupling efficiency of as high as −0.2 dB was achieved for a double-taper device with a tip width of 0.4 μm and total length of 85 μm.
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1. Introduction

In the development of functions in communication devices and systems along with maturing information technology, all components of the communication system are expected to have higher performances owing to the enhancements in high-quality data service and Internet of things (IoT) technology.[1] Because a simple modulation system of on–off keying (OOK) cannot accommodate the demanded capacity of optical communications, several technologies, such as wavelength division multiplexing (WDM), multilevel modulation, phase shift keying (PSK), and their combinations have been introduced,[2–11] which require a complicated transceiver configuration and consume a large amount of power.

One of the solutions to overcome these problems is introducing an integration of optical communication devices.[12–14] Developing a module form by discrete optical devices requires the construction of free-space interconnection with manual-fine adjustment at the submicrometer level to realize highly efficient coupling between them.[15,16] An increase in the number of components for complex communication system means an increment in the number of alignment points. In addition, each device has power margins for high versatility and the summation of power margins leads to large wasted power. By realizing monolithic integration of optical components, no alignment exists in the chip, and an optimal system in terms of power consumption can be built.[17]

In the fabrication of large-scale photonic-integrated circuits (PICs), silicon (Si) is a very attractive material owing to the availability of a large-diameter wafer and manufacturability through CMOS process equipment. Because this material is transparent for a wavelength range of 1.3–1.6 μm, which is used in low-loss optical fiber communications, various passive devices have been developed on a Si platform in the field of Si photonics. However, it is difficult to obtain light emission from a Si-based material owing to its indirect bandgap property. Many studies have focused on Si light sources for communication but their results are not adequate to ensure practical use from the viewpoint of efficiency and output power.[18,19]

So far, three main types of solutions have been reported to integrate light sources on a Si platform. The first solution is a butt-coupling method between active devices and Si photonics chip, which are fabricated discretely.[20,21] In this method, high quality and reliable chips are available as long as coupling loss can be compensated. The second involves heteroepitaxial growth on a Si substrate. InP-based materials are grown on a Si wafer for use in optical communication systems; however, this leads to generation of anti-phase domains and cracks, and sufficient optical characteristics cannot be obtained owing to the difference in lattice constants. Metamorphic growth techniques with off-cut or patterned Si substrates have also been investigated as solutions. Recently, some research groups utilized quantum dot layers on GaAs, which might have higher defect tolerance, and a lasing operation with fairly low threshold current as well as moderately high reliability was achieved.[22,23] This technology can be used for InP-based PICs on a large-diameter Si wafer, however, this has not been demonstrated on a silicon-on-insulator (SOI) wafer with Si waveguides because this technology is sensitive to surface condition and requires a thick buffer layer between the active layer and Si layer, which makes effective optical coupling difficult. The third method introduces a bonding technology.[24–27] Compared with the heteroepitaxial growth method, the wafer-bonding technology can ignore the lattice mismatch and thus eliminates the need for the thick buffer layer.

Our group also reported III–V/SOI hybrid devices with ring-resonator-type mirrors or AlInAs-current confinement structure by utilizing N_2 plasma activated bonding, which requires relatively low temperatures of 150 °C for the bonding process and can suppress damage to the active layer.[28,29] For multi-functional PICs, not only lasers but also detectors and amplifiers are required. Besides, because the optical mode shapes between III–V hybrid islands and Si waveguides are quite different and such a PIC chip involves a large number of connecting points, high efficiency coupling between them is critical. Owing to the different mode shape, a butt-coupling structure generates relatively large scattering at the interface. To avoid this, a double-taper-type structure should be introduced. The improvement of the coupling efficiency and assured fabrication processes of the taper structure are key issues in hybrid PICs. Some research groups introduced a Si waveguide thickness larger than 350 nm or

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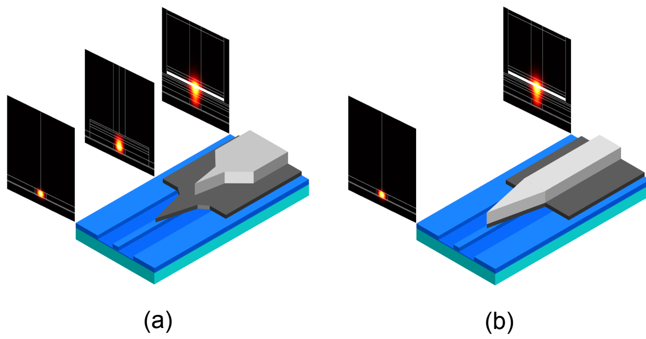

Fig. 1. (Color online) Schematics of taper couplers: (a) double-taper structure and (b) single-taper structure.

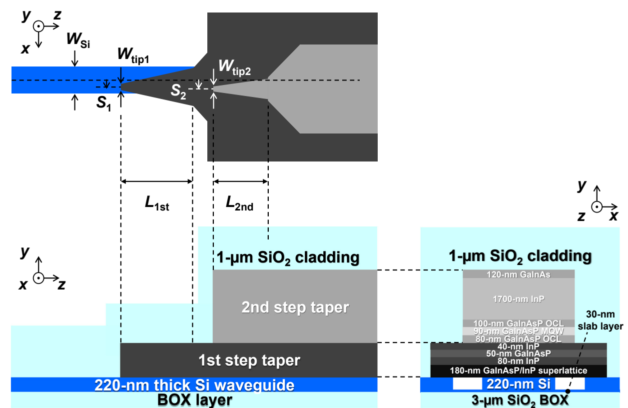

Fig. 2. (Color online) Parameters of double-taper-type coupler.

Table I. Layer structure of double-taper coupler.

Layer name	Material composition	Layer thickness	Taper level
p-Contact	$Ga_{0.47}In_{0.53}As$	120 nm	2nd
p-Cladding layer	InP	1700 nm	2nd
Upper u-OCL	$Ga_{0.22}In_{0.78}As_{0.47}P_{0.53}$	100 nm	2nd
TS0.15% barrier × 5	$Ga_{0.25}In_{0.75}As_{0.50}P_{0.50}$	10 nm	2nd
CS1.07% well × 5	$Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$	6 nm	2nd
TS0.15% barrier	$Ga_{0.25}In_{0.75}As_{0.50}P_{0.50}$	10 nm	2nd
Lower u-OCL	$Ga_{0.22}In_{0.78}As_{0.47}P_{0.53}$	80 nm	2nd
n-InP ES	InP	40 nm	1st
n-GaInAsP contact	$Ga_{0.22}In_{0.78}As_{0.47}P_{0.53}$	50 nm	1st
n-InP contact	InP	80 nm	1st
u-InP/GaInAsP SL (6 nm/7 nm × 14 pairs)	$InP/Ga_{0.22}In_{0.78}As_{0.47}P_{0.53}$	180 nm	1st
Top Si	Si	220 nm	—
BOX	SiO_2	3 μm	—
Si Substrate	Si	350 μm	—

inserted the intermediate layer at the bonding interface to increase the coupling efficiency;[30] however, these limit the design flexibility of the photonic devices. Thus, in this study, we designed and validated a high coupling efficiency double-taper optical coupler with 220-nm-thick Si waveguide, which is the thickness usually employed in Si photonics wave-guides, without an intermediate layer.

2. Design of taper structure

Figure 1(a) shows a schematic of the proposed double-taper-type couplers. For comparison, a conventional single-step taper structure employed in a previous work on hybrid lasers[28] is shown in Fig. 1(b). Although the single-step taper structure can achieve high coupling efficiency, it requires a relatively long length and causes insufficient current injection to the taper. This insufficient current injection results in saturable absorption effect in the hybrid lasers. In the proposed double-step structure, the introduction of an additional taper reduces the difference in equivalent refractive indices, which leads to a shorter length. Subsequently, a larger apex angle of the taper can be adopted, which results in a shorter length even though it needs two taper sections. Figure 2 shows the schematic of the double-taper structure. The design parameters used in this investigation include the width of Si waveguide, W_{Si}, lengths of the tapers, L_{1st} and L_{2nd}, tip widths of the tapers, W_{tip1} and W_{tip2}, and the misalignments between the Si waveguide and the tapers, S_1 and S_2. Table I describes the layer structure used in this design process. The layer structure is the same as that of the hybrid laser, but no absorption is considered in the calculations. The finite difference method was used in the following simulation, and the coupling efficiency was calculated with the fundamental mode.

2.1 Si waveguide width and first step taper

First, the coupling efficiency between the Si waveguide and III–V island in the first-taper structure is discussed. Figure 3 shows the effect of the first taper length L_{1st} on the coupling efficiency for various Si waveguide widths W_{Si} where S_1 and W_{tip1} are assumed to be 0. This indicates that the narrow Si waveguide corresponds to a high coupling efficiency with a short taper length. Figure 4 shows the effect of the tip width W_{tip1} on coupling efficiency for $L_{1st} = 100$ μm and almost the same tendencies are noted except in the case of $W_{Si} = 3$ μm. The difference in $W_{Si} = 3$ μm is caused by a shortage of taper length as shown in Fig. 3 where the coupling efficiency with $W_{Si} = 3$ μm does not saturate enough even with $L_{1st} = 100$ μm. The Si waveguides with widths of 1 and 1.5 μm have a larger tolerance of the tip width for the coupling efficiency. Although the tip width should ideally be 0, the scenario is impractical owing to the resolution limit of the lithography.

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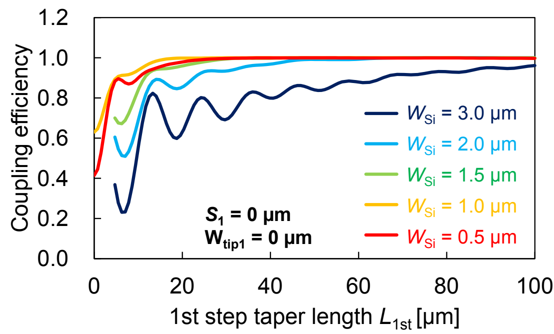

Fig. 3. (Color online) Effect of first step taper length L_{1st} on coupling efficiency for various Si waveguide widths W_{Si} for $W_{tip1} = 0$ and the misalignment $S_1 = 0$.

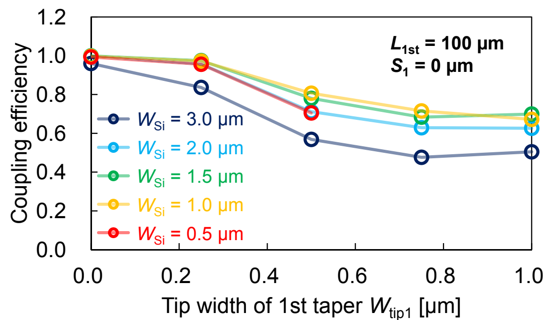

Fig. 4. (Color online) Effect of tip width of first taper on coupling efficiency for various Si waveguide widths for $L_{1st} = 100$ μm and $S_1 = 0$.

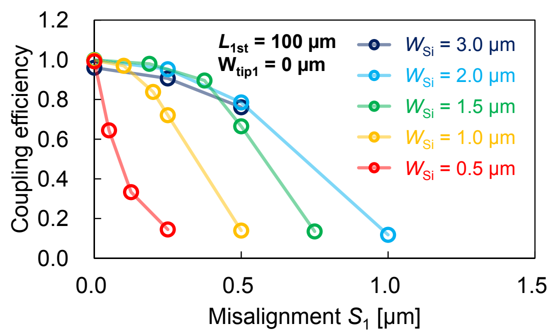

Fig. 5. (Color online) Effect of misalignment of first taper on coupling efficiency for various Si waveguide widths for $L_{1st} = 100$ μm and $W_{tip1} = 0$.

Therefore, a large tolerance of the tip width is important to avoid variations in the tip width due to lithographic errors. Figure 5 shows the effect of misalignment S_1 on the coupling efficiency for $L_{1st} = 100$ μm. As can be seen, because the coupling efficiency decreases rapidly in narrower Si waveguides, the allowable misalignment also rapidly decreases with the Si waveguide width. However, because a 1.5-μm Si waveguide width indicates a tendency similar to that for 2 and 3 μm in terms of the coupling efficiency, $W_{Si} = 1.5$ μm should be selected to ensure a larger tolerance in misalignment. Moreover, for $W_{Si} = 1.5$ μm, the first step taper should be more than 40 μm, as shown in Fig. 3.

2.2 Second step taper

Next, we discuss the design of the second-taper coupler. In the following investigation, the values for length L_{1st}, tip width W_{tip1}, Si waveguide width W_{Si}, and misalignment S_1 of the first taper are set as 100, 0, 1.5, and 0 μm, respectively.

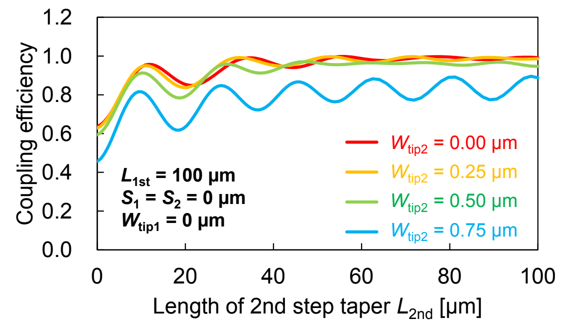

Fig. 6. (Color online) Effect of second step taper length on coupling efficiency for various Si waveguide widths for $L_{1st} = 100$ μm, $S_1 = S_2 = 0$, and $W_{tip1} = 0$.

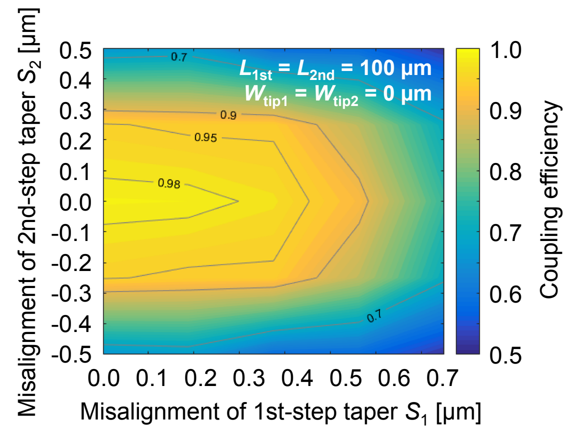

Fig. 7. (Color online) Contour map of coupling efficiency for misalignments of first and second step tapers.

Figure 6 shows the calculated coupling efficiency as a function of the second-taper length L_{2nd} for various tip widths W_{tip2}. Similar to that in the single taper case shown in Fig. 3, a narrower tip width provides higher coupling efficiency. A tip width of 0.25 μm shows almost the same performance as that for 0 μm, which means that a certain broadening of the tip width is acceptable.

Then, we focus on the effect of the misalignments of the first and second tapers on the coupling efficiency. Because the first and second tapers are patterned separately, the combination of the two misalignments are considered. Figure 7 shows a contour map of the coupling efficiency as a function of these misalignments. The map becomes symmetric along the line of $S_2 = 0$, which means that the same coupling efficiencies are obtained with the same amount of misalignment regardless of the shift direction of the second step taper even when the first step taper has a shift of $+x$-direction. The reason for the symmetric map is that the calculated coupling efficiency includes only the fundamental mode and the related optical mode is the same even in a shift of $-x$- and $+x$-directions. The tendencies are almost the same with less than 0.2-μm misalignment of the first step taper.

Finally, the tolerances of alignment and tip width are determined with the combination of the two tapers. By using the results shown in Figs. 3 and 6, the length of the first and the second tapers, that is, L_{1st} and L_{2nd} are set as 40 and 34 μm, respectively. Then, structural dependences of the tip width and the misalignments are calculated. Figure 8 shows

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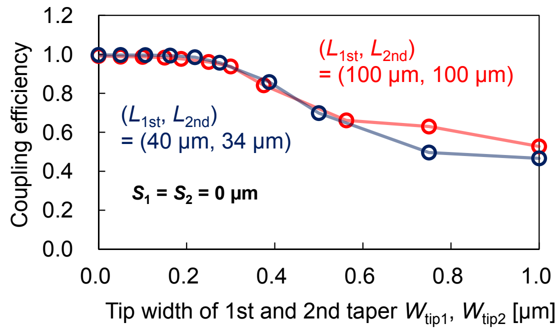

Fig. 8. (Color online) Effect of tip width of first and second step tapers on coupling efficiency for different taper lengths.

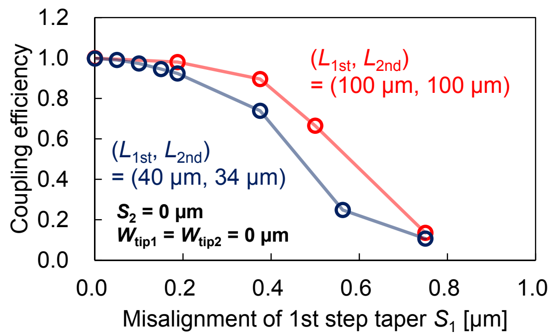

Fig. 9. (Color online) Effect of misalignment of first step taper on coupling efficiency for different taper lengths for $S_2 = 0$, and $W_{tip1} = W_{tip2} = 0$.

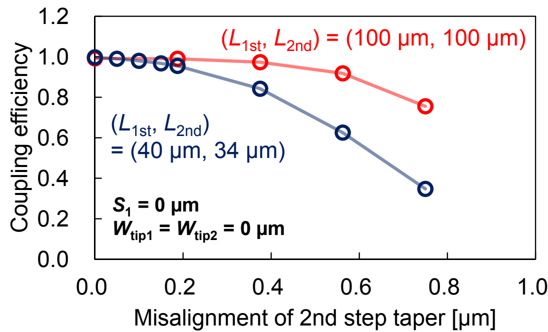

Fig. 10. (Color online) Effect of misalignment of second step taper on coupling efficiency for different taper lengths for $S_2 = 0$, and $W_{tip1} = W_{tip2} = 0$.

the effect of the tip widths W_{1st} and W_{2nd} on the coupling efficiency, where the tip widths of the first and the second taper are assumed to be the same owing to the resolution limit of the lithography technology used. As can be seen, both the taper structures demonstrate nearly the same tendencies for tip widths less than 0.5 μm, which means that the degradation of the coupling efficiency owing to the use of a wide tip width cannot be compensated by using a long taper length.

Figures 9 and 10 show the effect of the misalignments S_1 and S_2 on the coupling efficiency. Compared with the tendency of the second-taper misalignment S_1, the coupling efficiency is sensitive to the misalignment of the first taper S_1. The reason is that the first taper is connected to the Si waveguide where light is strongly confined, and the optical mode width is narrow, whereas the second taper is coupled to the III–V/Si waveguide with relatively wide optical mode.

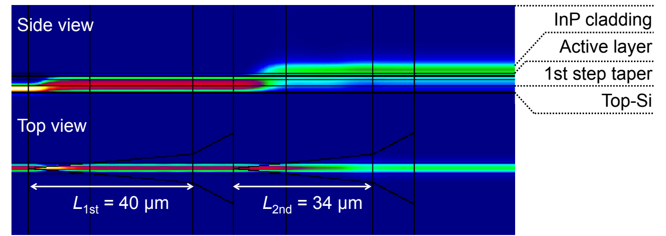

Fig. 11. (Color online) Optical mode profile of the designed double-taper coupler.

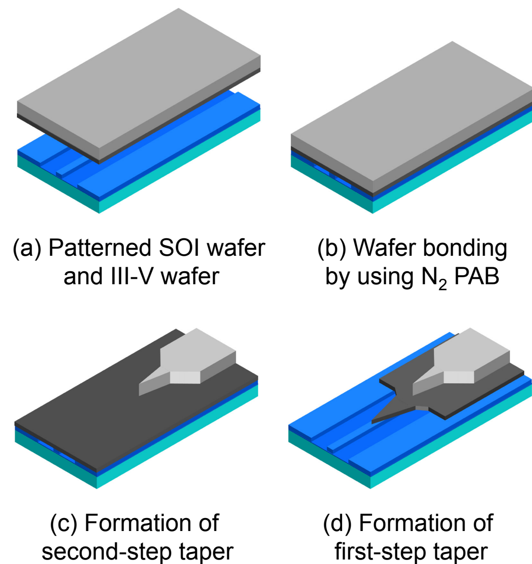

Fig. 12. (Color online) Fabrication process of the hybrid devices for evaluation of taper structure.

Owing to the difference in the optical mode, the coupling efficiency is maintained until the misalignment of 0.2 μm in the second taper. In contrast to the short taper, a taper length of 100 μm provides high coupling efficiency until a misalignment of 0.4 μm owing to the decreased apex. The short taper exhibits a smaller tolerance in misalignment, but a misalignment of less than 0.1 μm leads to an acceptable coupling efficiency even with the short taper, the value of which is within the alignment accuracy of conventional lithography steppers.

Figure 11 shows the calculated optical mode field of the designed taper structure (the first and the second tapers are 40 and 34 μm, respectively) with tip widths of 0 μm and misalignments of 0 μm. As seen in the figure, the coupling to the III–V layer was confirmed.

3. Fabrication

Figure 12 shows the fabrication process of the hybrid device developed to investigate the taper structure. First, an SOI wafer with Si waveguide and GaInAsP/InP wafer containing the layers listed in Table I were prepared [Fig. 12(a)] by organo-metallic vapor phase epitaxy (OMVPE). However, to evaluate the coupling efficiency, the well and barrier layers specified in Table I were replaced by a GaInAsP bulk layer (the bandgap wavelength is 1.2 μm), which was transparent till 1.55 μm and directly bonded using the N_2 plasma-activated bonding technology [Fig. 12(b)]. The Si waveguide was drawn by using electron beam lithography with ZEP-

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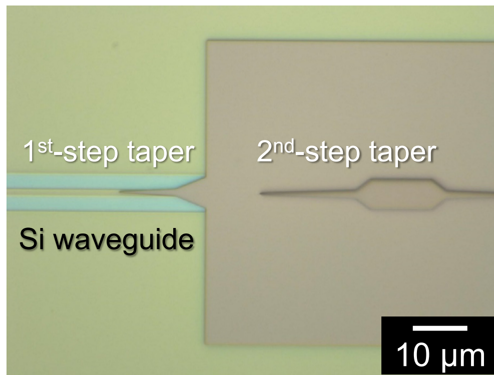

Fig. 13. (Color online) Optical microscopic top view of the fabricated taper.

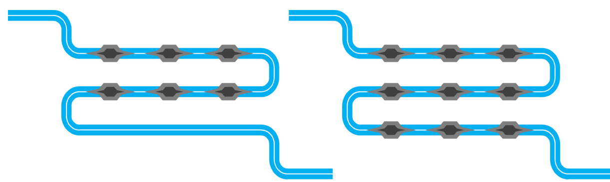

Fig. 14. (Color online) Schematic of fabricated photonic circuits.

520A and the temperature during the bonding process was 150 °C. After the removal of the InP substrate by wet chemical etching with HCl solution, an island pattern with a second-taper was formed by using photolithography with a conventional i-line stepper. The pattern was transferred to the III–V layer by inductively coupled plasma-reactive ion etching (ICP-RIE) with a mixture gas of CH_4, H_2, and Cl_2 [Fig. 12(c)]. The height of the second taper was controlled by changing the dry-etching time. Then, the island pattern with first-taper was formed in the same way as the former island and transferred to the III–V layer by RIE with a mixture gas of CH_4 and H_2. Next, the Si surface was cleaned with HCl and BHF solution to remove the residual III–V materials and amorphous layer at the bonding interface.[31] After the SiO_2 cladding was deposited on the Si waveguides and the III–V islands using plasma-enhanced chemical vapor deposition (PECVD), the cleavage facets were formed after making grooves by using a dicing saw machine.

In this work, each taper tip width (W_{tip1}, W_{tip2}) was changed between 0–0.6 μm. It should be noted that W_{tip} indicates not the fabricated width but the width of the mask design used in photolithography.

Figure 13 shows a microscopic top view of the fabricated taper structure. Two sharp tips and accurate alignment could be observed. Figure 14 shows a schematic top view of the fabricated photonic circuits. All waveguides had the same length (total length between the input and the output ends was 3 mm), but a different number of III–V islands. By comparing the transmission power and the number of III–V islands, we could obtain the coupling efficiency of the double-taper coupler.

4. Measurement and discussion

In the measurement, an amplified spontaneous emission (ASE)-type optical source was used, and incident light was controlled into a TE-like mode by using a polarization splitter and a polarizer. To extract its characteristics at a wavelength

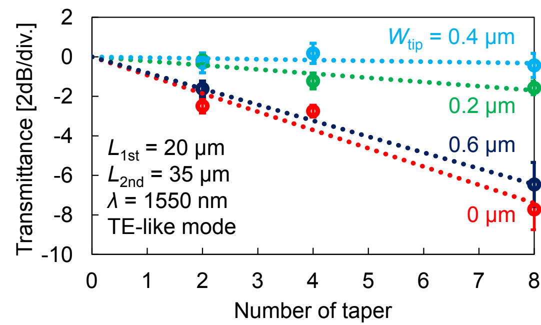

Fig. 15. (Color online) Effect of number of tapers on transmission.

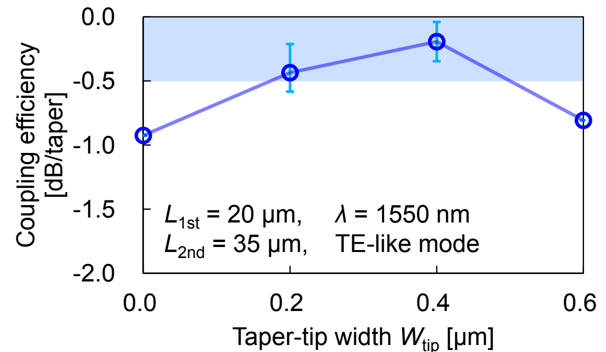

Fig. 16. (Color online) Effect of tip width on coupling efficiency.

of 1550 nm, we used transmission light having an average wavelength of 1548–1552 nm.

Figure 14 shows the transmission intensity as a function of the number of tapers. In this measurement, the first- and second-taper lengths were 20 and 35 μm, respectively, and the same tip width for both tapers was used ($W_{tip1} = W_{tip2}$). The tapers with other lengths were also fabricated but we could not obtain sufficient data for the characterization owing to fabrication errors. Because the transmission power reduced when the number of tapers was increased, we derived the coupling efficiency from the slope of the fitting line. Because one island section contains two double-taper couplers, the number of tapers is two times the number of islands, as shown in Fig. 15. The best data for each design are shown in the figure. It was determined that the angles of the slopes did not change monotonically, and $W_{tip} = 0.4$ μm demonstrated the smallest angle and the highest coupling efficiency.

Figure 16 shows the effect of W_{tip} on the coupling efficiency. Three photonic circuits with the same structure were fabricated and measured simultaneously. A coupling efficiency of as high as −0.2 dB was obtained with $W_{tip} = 0.4$ μm and a total length of 85 μm. The coupling efficiency was derived by applying the average in obtained coupling efficiencies. The reason why coupling efficiency with $W_{tip} = 0.4$ μm was superior was low etching reproducibility during the transfer of pattern to the SiO_2 hard mask and III–V layers. Although $W_{tip} = 0$ μm provided the best results in the calculation, the scenario was impractical because $W_{tip} = 0$ μm was beyond the lithography resolution limit. Some of the tapers had a saw-tooth shape at the tip area. A double-taper coupler with a coupling efficiency of higher than −0.5 dB was achieved even with a thin top-Si layer of width 220 nm and no interlayer at the bonding interface.

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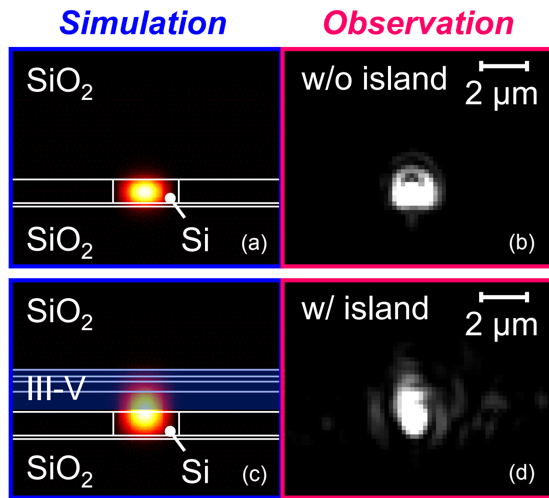

Fig. 17. (Color online) Comparison of near field pattern between with and without a III–V island.

Figure 17 shows a comparison of simulated optical mode fields and observed near field pattern in Si waveguide and III–V/SOI hybrid part. As the near field pattern at III–V/SOI hybrid part had a vertically long shape, it was confirmed that the light was coupled to III–V layers.

5. Conclusions

In this work, a highly efficient double-taper coupler between the III–V/SOI hybrid part and the Si waveguide was designed and validated. In the design of the double-taper structure, it was found that a 1.5-μm-wide Si waveguide can help achieve both a shorter taper length and a large misalignment tolerance. Further, a 40-μm-long first taper and 34-μm-long second taper leads to a high coupling efficiency of more than −0.2 dB/taper and a sufficient misalignment tolerance of ±100 nm.

The double-taper couplers with narrow tips were successfully fabricated and a high coupling efficiency of 0.2 dB/taper with the 220-nm-high Si waveguide was obtained without any intermediate layer. The high coupling efficiency can lead to improvement in the III–V/SOI hybrid integrated devices and can be expected to realize an efficient hybrid PICs.

Acknowledgments

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