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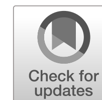

Effect of increasing gate capacitance on the performance of a p-MoS_2/HfS_2 van der Waals heterostructure tunneling field-effect transistor

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We propose a p-MoS_2/HfS_2 van der Waals (vdW) heterostructure tunneling field-effect transistor (TFET) with a type-II band alignment for future power-efficient electronics. The differences in temperature dependence between p-MoS_2/HfS_2 TFET and HfS_2 metal-oxide-semiconductor field-effect transistor showed that the turn-on current of p-MoS_2/HfS_2 TFET originated from band-to-band tunneling. To suppress the impact of interface traps, reduce the subthreshold swing (SS), and increase the gate capacitance, the 25 nm Al_2O_3 gate dielectric was replaced with a 15 nm HfO_2 layer. Additionally, a buried Ni back-gate structure was introduced to reduce the area of overlap between the gate, contact electrodes, and gate leakage along with the scaling of equivalent oxide thickness. Subsequently, enlargement of gate capacitance by three times led to the reduction of SS from 700 to 300 mV dec^{-1}, which verified that increasing the gate capacitance suppressed the impact of interface traps and improved gate controllability in the vdW heterostructure TFET. © 2019 The Japan Society of Applied Physics

1. Introduction

Moore's law of scaling down transistors has been the backbone of the semiconductor industry.[1,2] The transistor density in integrated circuits (ICs) has increased by four orders of magnitude in the past half century, whereas the price per transistor has decreased by six orders owing to the miniaturization of semiconductor devices. However, these merits of scaling are accompanied by tremendous increase in power consumption, which is one of the most serious issues to be solved.[3] An option to reduce the switching power dissipated by complementary metal-oxide-semiconductor-based ICs is to lower the operating voltage, V_{DD}. Nevertheless, in the subthreshold region of conventional metal-oxide-semiconductor field-effect transistors (MOSFETs), the thermionically distributed electrons at source entail that at least 60 mV is necessary to drive the current by one order of magnitude at room temperature. In other words, the subthreshold swing (SS) that accounts for the inverse of the derivative of the subthreshold slope should have a minimum value of 60 mV dec^{-1}.[4] To reduce the operating voltage without any performance loss, the turn-on steepness should be increased to break through the 60 mV dec^{-1} bottleneck for future power-efficient electronics.[5] A tunneling field-effect transistor (TFET) is a possible alternative to a MOSFET because the carrier injection of a TFET is originated by band-to-band tunneling (BTBT), which does not depend on the thermal process.[6] Extensive research on heterojunction TFETs using conventional bulk materials resulted in BTBT injection and steep slope operation.[7,8] However, these TFETs suffered from trap states and lattice mismatch at the tunneling interface.[9] Thus, a defect-free tunneling interface with an abrupt band edge is crucial for high-performance TFETs.

To overcome the limitation induced by these intrinsic defects, novel materials should be exploited to form superior tunneling junctions.[10–12] Transition metal dichalcogenides (TMDs), representing a large part of two-dimensional materials, showed a great potential because of the dangling bond-free surface and steep band edge due to the layered crystal structures.[13–15] Reference 16 demonstrated the BTBT in a stacked WSe_2/MoS_2 heterostructure, where this device showed a clear negative differential resistance below 175 K. Reference 17 proposed a $SnSe_2$/WSe_2 heterostructure TFET by observing an average SS of 80 mV dec^{-1} for exceeding two decades of drain current with a minimum of 37 mV dec^{-1} at room temperature. Reference 18 reported a TFET combined with highly-doped germanium and bilayer MoS_2, with an average SS of 31.1 mV dec^{-1} for four decades and a minimum of 3.9 mV dec^{-1} at room temperature. Tunneling junction formed with TMDs could produce an atomically abrupt interface with large tunneling area and suppressed trap states.[19] However, an electrostatic doping required an extra gate electrode to modulate the carrier concentration at source, which lead to the complexity in structure. Thus, a traditional p^+-n^--n^+ three-terminal TFET composited of controllable source carrier concentration and conventional high-κ oxide is demanded for the practical application of TMD-based TFET.

In this study, we fabricated a TFET by stacking Nb-doped MoS_2 on HfS_2 to construct a vertical van der Waals (vdW) heterostructure.

The MoS_2 doped with niobium was reported to be controllable in hole concentration without band renormalization, and the p-MoS_2/HfS_2 vdW heterostructure transistor was the first implementation of TFET using a substitutional doped source in 2D materials.[20] The valence band maximum of MoS_2 and the conduction band minimum of HfS_2 were estimated to be −5.86 eV and −5.10 eV, respectively, by density functional theory calculations.[21] The band alignment of MoS_2 and HfS_2 lead to a Type-II heterointerface with small band gap overlap, which enhanced the BTBT injection due to the relatively lower tunneling barrier and shorter tunneling distance.[22] The back-gate bias controlled the Fermi level of HfS_2 and made an overlap between the MoS_2 source valance band and channel conduction band. Then, the electron from the valence band of MoS_2 started to tunnel into the empty states in the conduction band of HfS_2, which switched the transistor from off-state to on-state. We demonstrated the p-MoS_2/HfS_2 vdW TFET and how the gate dielectric affected its performance.[23,24] In this paper, we would like to summarize and give a systematic illustration of the p-MoS_2/HfS_2 vdW TFET with solutions to recent challenges to improve the performance.

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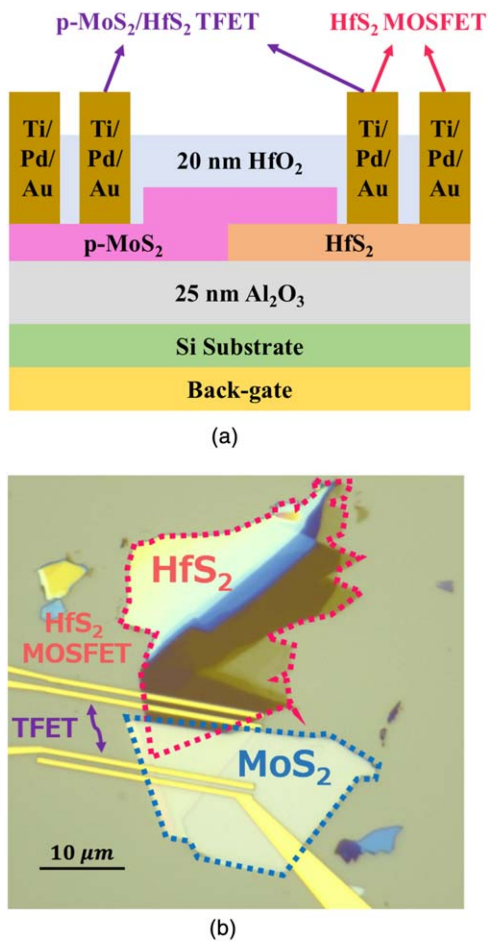

Fig. 1. (Color online) Brief structure of the global back-gate p-MoS_2/HfS_2 vdW TFET with 25 nm Al_2O_3 gate dielectric. (a) Schematic view. (b) Optical microscope image.

2. Experimental methods

The typical device we fabricated to characterize the heterostructure was p-MoS_2/HfS_2 vdW TFET in a global back-gate structure with 25 nm Al_2O_3 as the gate dielectric and degenerately doped Si substrate as the gate electrode. Figure 1(a) shows the schematic view of the 25 nm Al_2O_3 p-MoS_2/HfS_2 vdW TFET, and Fig. 1(b) shows the optical microscope image of the fabricated device. The back-gate dielectric of 25 nm Al_2O_3 was deposited on n^+-Si substrate by performing 300 cycles of plasma-enhanced atomic layer deposition (ALD) at 250 °C with trimethylaluminum. HfS_2 flakes were exfoliated and transferred to the substrate by scotch-tape method. On the other hand, MoS_2 flakes were first transferred to the polydimethylsiloxane (PDMS), and then transferred onto target HfS_2 flakes by viscoelastic stamping method. It was taken care of that once both flakes were in contact, the stamp was not pressed further and the PDMS was peeled off slowly, which made sure of higher success yield and heterostructure quality.[25] After the heterostructure formation, S/D electrodes were designed by electron beam lithography (EBL) and Ti/Pd/Au (20 nm/20 nm/60 nm) were deposited using electron beam evaporation for the contact metal. As shown in Fig. 1(b), both MoS_2 and HfS_2 flakes were characterized by a pair of electrodes to distinguish p-MoS_2/HfS_2 vdW TFET from HfS_2 MOSFET. After the lift-off process, 20 nm HfO_2 was deposited by thermal ALD using the precursors of Tetrakis(dimethylamino) Hafnium (TDMAH) and H_2O for 200 cycles at 150 °C to protect the device from atmospheric contaminants. After the back contact (Cr/Au: 20 nm/100 nm) deposition by electron beam evaporation, the device was annealed at 250 °C to improve the electrical performance.[26] The measurements were finally implemented in a vacuum chamber at 10^{-6} Torr at the temperature range from 295 to 200 K to investigate the temperature dependence of both the p-MoS_2/HfS_2 vdW TFET and HfS_2 MOSFET.

Even in a 2D material MOSFET, the SS was influenced by the interface trap as shown in Eq. (1).[27] The right term in brackets deteriorated the SS over 60 mV dec^{-1}. In 2D material-based TFET, it could also be speculated that the impact induced by interface traps contaminated the steepness of SS from the ideal condition. To mitigate the impact of interface traps C_{it}, one possible solution was to increase the gate capacitance C_{ox}, which could be implemented using high-κ dielectric or reducing the gate dielectric thickness. Therefore, we replaced the gate dielectric from Al_2O_3 (relative permittivity, ε_r, was extracted to be 9 in our experimental condition) to HfO_2 ($\varepsilon_r \approx 16$)

$$\mathrm{SS} = \frac{kT}{q} \ln 10 \cdot \left(1 + \frac{C_{it}}{C_{ox}}\right). \quad (1)$$

Before the fabrication of a p-MoS_2/HfS_2 vdW TFET with HfO_2 gate dielectric, we characterized the gate leakage in a general HfS_2 MOSFET with 10 nm HfO_2. The process flow was almost identical with the previous one but we replaced the gate dielectric with 10 nm HfO_2 deposited by ALD. The measurement results showed that the performance of this transistor was severely contaminated by the gate leakage (will be discussed in details in Sect. 3.2). As a result, a new device structure was required to minimize the influence of gate leakage and to investigate the subthreshold region of the transistors.

Figures 2(a) and 2(b) show the schematic view and the optical microscope image of the p-MoS_2/HfS_2 vdW TFET, respectively. In this structure, we utilized a Ni back-gate buried in the gate dielectric instead of a global back-gate, which dramatically decreased the overlapping area between S/D electrode and back-gate. To further reduce the gate leakage, the HfO_2 gate dielectric thickness was increased to 15 nm. The fabrication of substrates with buried Ni electrode began with the designing of gate electrode by EBL, followed by 50 nm Ni deposited on 90 nm SiO_2/n^{++}-Si substrate by electron beam evaporation. The remaining steps were almost the same as followed for the global back-gate structure after depositing 15 nm HfO_2 by plasma-enhanced ALD with 150 cycles of TDMAH followed by the dry etching of contact holes. Finally, the transistor was also measured in the vacuum chamber.

3. Results and discussion

3.1. Global back-gate p-MoS_2/HfS_2 vdW TFET with 25 nm Al_2O_3 gate dielectric

The p-MoS_2 source was doped with Nb of concentration 10^{19} cm^{-3}, and we confirmed that the Nb-doped MoS_2 was a p-type semiconductor even in a strong positive gate bias.[22] The transfer and output curves measured in vacuum are shown in Figs. 3(a) and 3(b). The on/off current ratio of the

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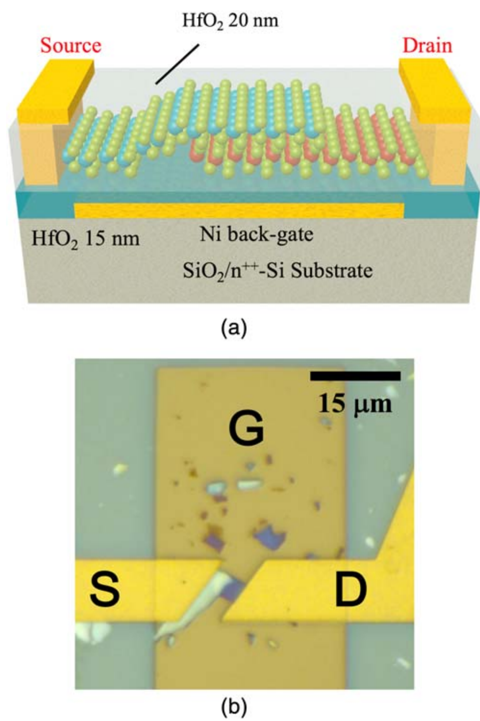

Fig. 2. (Color online) Device structure of p-MoS_2/HfS_2 vdW TFET using Ni electrode with 15 nm HfO_2 gate dielectric. (a) Schematic view. (b) Optical microscope image.

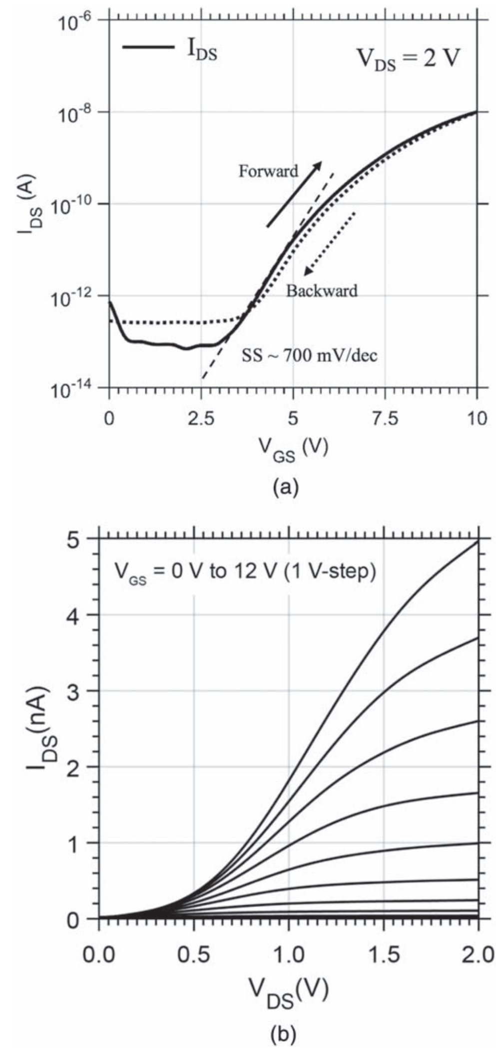

Fig. 3. Electrical characteristics of the global back-gate p-MoS_2/HfS_2 vdW TFET with 25 nm Al_2O_3 gate dielectric. (a) Transfer curves of the transistor at 2 V drain bias. (b) Output curves of the transistor at gate bias from 0 to 12 V (Step of 1 V).

p-MoS_2/HfS_2 vdW TFET was around 10^5, which enable the transistor to operate as an electrical switch. In the off-state, electrons from the valence band of MoS_2 were not able to move to the HfS_2 because there was no available state in HfS_2 due to the staggered gap of the heterojunction system. Only the minority drift current contributed to the off-state current so that the transistor could be switched off around 10^{-13} A due to the depletion of electrons and holes in MoS_2 and HfS_2. For a positive gate bias, the accumulation of electrons tuned the Fermi level of HfS_2 closer to the conduction band, whereas the Fermi level of MoS_2 did not shift much because of the high doping concentration. When the conduction band of HfS_2 was aligned with the valence band of MoS_2, the electrons started to tunnel from the valence band of MoS_2 to the empty states in the conduction band of HfS_2, which switched the transistor from off-state to on-state. The on-state current of the p-MoS_2/HfS_2 vdW TFET was over 10 nA measured at 2 and 10 V gate bias. We confirmed the p-type conduction of MoS_2 and rectified characteristics in our former experiments published in Ref. 23. In this trial of the TFET, we also confirmed the p-type conduction of MoS_2 by a pair of Ti/Pd/Au contacts, as shown in Fig. 1(b). When the back-gate voltage (VBG) was raised to a positive value, the slope of the current characteristic gradually reduced. Moreover, MoS_2 showed strong p-type conduction even at a positive gate bias over 10 V, resulting from heavy p-doping. By applying a negative bias to the HfS_2 terminal in TFET, the electrons diffused from the HfS_2 side to the MoS_2 side because the potential barrier was lowered. On the other hand, only a small reverse current flowed at a positive bias to the HfS_2 terminal because the tunneling window was switched off when gate bias was 0 V. Such a phenomenon was observed during the trial of this transistor as well. The minimum SS of this TFET was extracted to be around 700 mV dec^{-1}, which was not a satisfactory value and was possibly dependent on the trap states from sulfur vacancy, grain boundary, and interface between semiconductor and gate dielectric.[28–30]

To further characterize the p-MoS_2/HfS_2 vdW TFET and verify that the turn-on current was originated from BTBT, transfer curves of both the p-MoS_2/HfS_2 vdW TFET and HfS_2 MOSFET were measured from 295 to 200 K as shown in Fig. 1(b). Figures 4(a) and 4(b) show the temperature dependence of transfer curves for the HfS_2 MOSFET and p-MoS_2/HfS_2 vdW TFET, respectively. The minimum SS was also extracted, which is shown in Fig. 4(c). In the HfS_2 MOSFET, the electrons were injected from contact to the semiconductor channel through thermionic emission, so that we could get lower off-state current and steeper subthreshold slope at lower temperature. In contrast, the p-MoS_2/HfS_2 vdW TFET was weakly temperature dependent. The slight rising trend of the minimum SS was possibly caused by the difference between tunneling valleys. The highest valence band of bulk MoS_2 is at point Γ and the lowest conduction state of HfS_2 is at point M.[31,32] The momentum difference of wave number between the two valleys was compensated by phonons, and this speculation further proved that the turn-on current originated from the BTBT.

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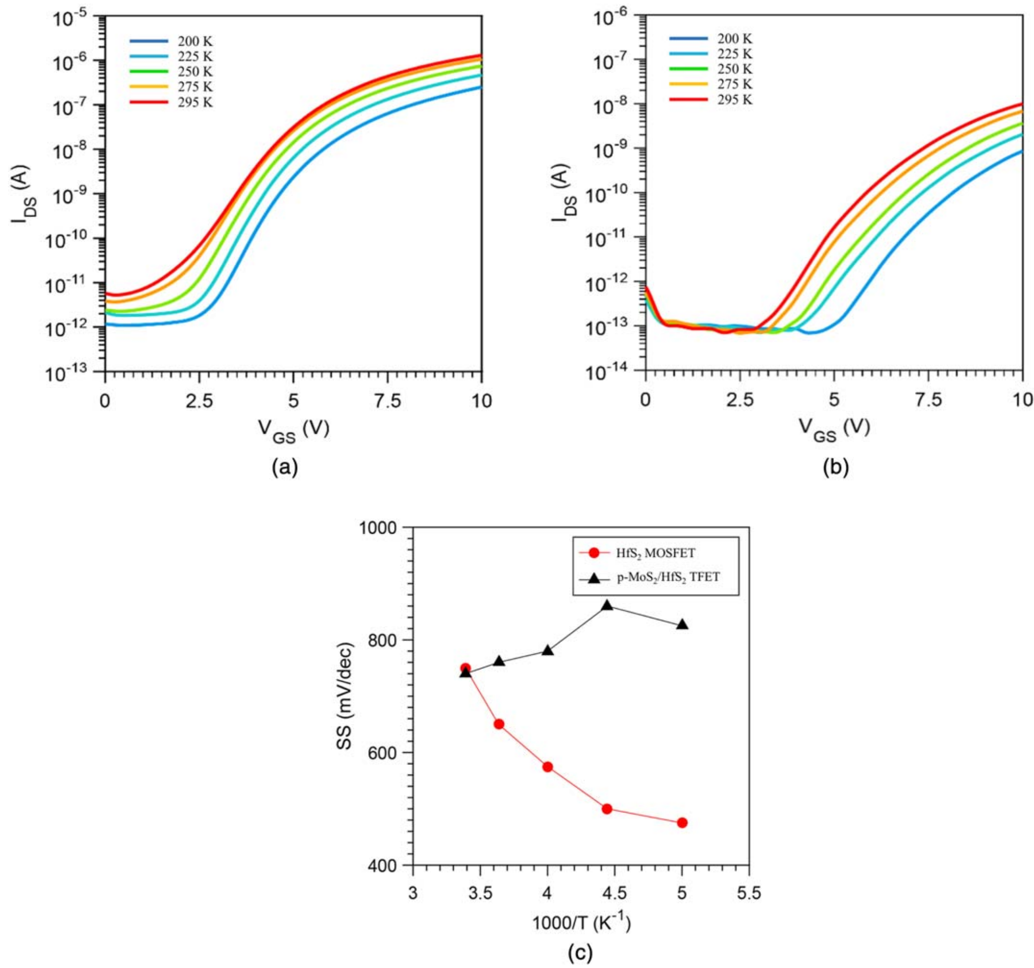

Fig. 4. (Color online) Temperature dependence of transfer curves of HfS_2 MOSFET and p-MoS_2/HfS_2 vdW TFET (295−200 K). (a) HfS_2 MOSFET. (b) p-MoS_2/HfS_2 vdW TFET. (c) Minimum SS plotted as a function of 1000/T extracted from (a) and (b).

3.2. Gate leakage characterization and interface trap density estimation in HfS_2 MOSFET

As discussed in Sect. 2, to replace the gate oxide with thin high-κ dielectric, we fabricated a global back-gate HfS_2 MOSFET with 10 nm HfO_2 gate dielectric to characterize the gate leakage. Figures 5(a) and 5(b) show the schematic view and the optical microscope image of the fabricated transistor, respectively. As shown in Fig. 5(c), the subthreshold characteristics were obscured by the gate leakage, which deteriorated the on/off ratio and hindered the observation of the true subthreshold slope of the transistor. In detail, the edge length of the S/D measuring pads was designed to be 70 μm, and the overlapping between S/D electrodes and back-gate was evaluated to be 9800 μm^2, which provided parasitic current paths for gate leakage current as shown in Fig. 5(a). The potential drop between drain electrode and back-gate was 2 V with an initial gate voltage at 0 V, where the gate leakage over 10 nA was several orders of magnitude larger than the subthreshold current. Hence, it was necessary to reduce the gate leakage below the subthreshold current to observe the true subthreshold slope.

Furthermore, to evaluate the interface of HfS_2/Al_2O_3 and HfS_2/HfO_2, we simply estimated the interface trap density, D_{it}, from Eq. (1), where D_{it} was extracted by C_{it}/q, here q represents the elementary charge. The SS of HfS_2 MOSFET with 25 nm Al_2O_3 was around 700 mV dec^{-1} as shown in Fig. 4(a), and with 10 nm HfO_2 was 200 mV dec^{-1} as shown in Fig. 5(c), which means that the interface trap density, D_{it}, of HfS_2/Al_2O_3 and HfS_2/HfO_2 were 2.12×10^{13} cm^{-2} eV^{-1} and 2.06×10^{13} cm^{-2} eV^{-1}, respectively. The interface traps deteriorated the SS several times larger than the ideal value of 60 mV dec^{-1}. Additionally, the SS of a vdW TFET also degraded due to the poor efficiency to modulate the channel electron concentration because of interface traps.

According to Eq. (1), the SS of HfS_2 MOSFET should linearly change with decreasing temperature. However, in our experimental results from Fig. 4(c), the SS increased exponentially as the temperature increased from 200 to 295 K. One possible reason is that the HfS_2 flake was not thin enough to show strong electrostatics, which could be another reason for the deterioration of the SS of HfS_2 MOSFET. We used a transmission electron microscope to confirm that the HfS_2 flake thickness of the sample in Fig. 1(b) was over 10 nm. In Fig. 6, we divided the current path into path-1 and path-2. Current path-1 at the bottom layers of the flakes was well-controlled by the back-gate, whereas it was difficult to control current path-2 at the top layers using the back-gate. Therefore, the intrinsic carrier in path-2 increased exponentially when the temperature increased, which contributed to higher off-state current and degraded SS. We believe that thinner flakes will enhance the gate controllability towards a steeper subthreshold slope.

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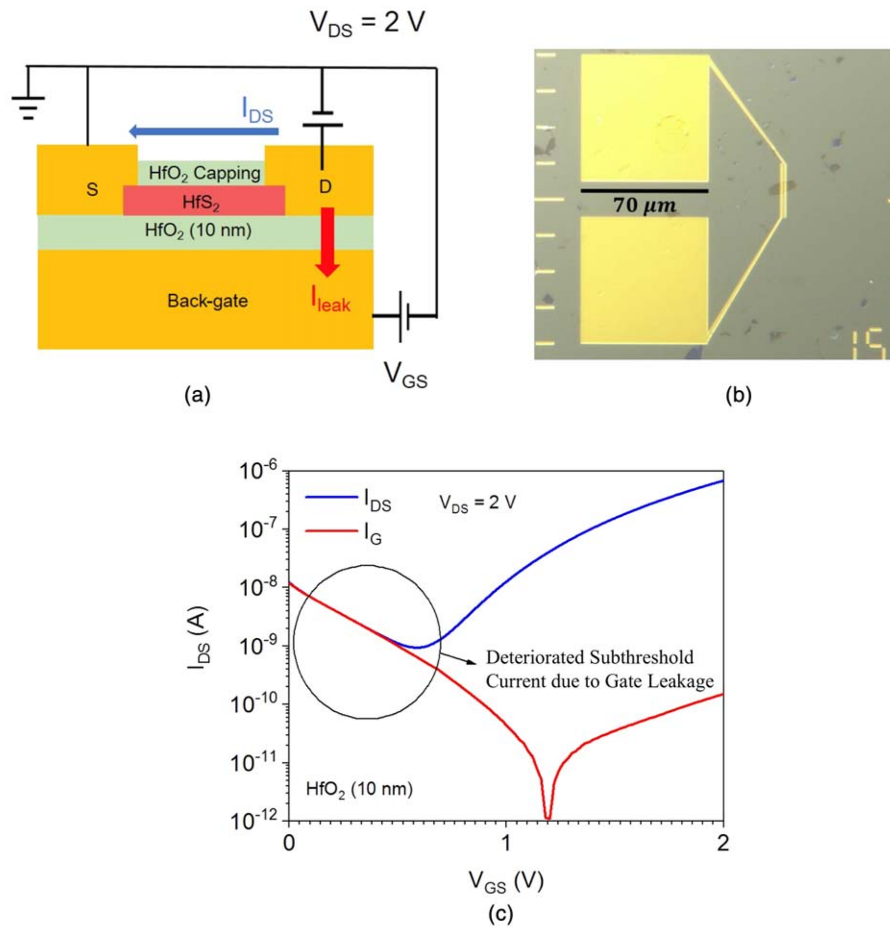

Fig. 5. (Color online) Gate leakage characterization in HfS_2 MOSFET with 10 nm HfO_2 gate dielectric. (a) Schematic view of the fabricated transistor. The blue and red arrows represent the paths of channel current and gate leakage. (b) Optical microscope image of the fabricated transistor. The edge length of measuring pads was designed to be 70 μm. (c) Transfer curves of the fabricated transistor. Blue and red curves represent the measured channel current and gate leakage. The circled region was contaminated by gate leakage.

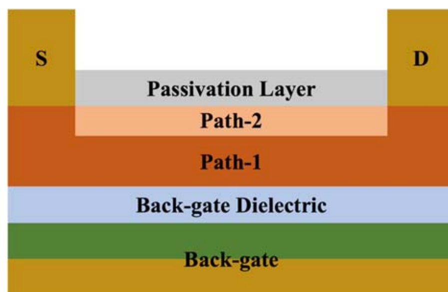

Fig. 6. (Color online) Brief schematic view of a HfS_2 MOSFET. The current path in the HfS_2 channel is divided into path-1 and path-2. Current path-1 at the bottom layers is well-controlled by the back-gate, but current path-2 at the top layers is difficult to control using the back-gate.

3.3. p-MoS_2/HfS_2 vdW TFET using a Ni electrode buried in 15 nm HfO_2 gate dielectric

As discussed above, the large overlapping between S/D electrode pads and back-gate caused the high gate leakage. Thus, we utilized a Ni electrode as a back-gate buried in the HfO_2 gate dielectric. It could be evaluated that the overlapping between S/D electrodes and gate electrode was around 300 μm^2 as shown in Fig. 2(b), which reduced by 97% compared to the former case of the global back-gate structure. We simultaneously increased the HfO_2 thickness to 15 nm to further suppress the gate leakage. As a result, the introduction of 15 nm HfO_2 (equivalent oxide thickness or EOT = 3.7 nm) lead to three times increase in the gate capacitance compared to the previous 25 nm Al_2O_3 (EOT = 10.8 nm). The transfer curves measured in vacuum are shown in Fig. 7. The gate leakage current was suppressed around 10^{-13} A by increasing the oxide thickness by 5 nm and reducing the overlapping by 97%. As a result, the transistor showed on/off ratio beyond 10^4 with the minimum

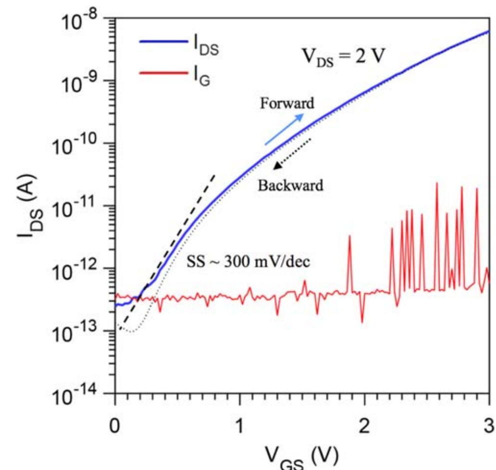

Fig. 7. (Color online) Electrical characteristics of the p-MoS_2/HfS_2 vdW TFET using Ni electrode with 15 nm HfO_2 gate dielectric. Blue and red curves represent the measured channel current and gate leakage.

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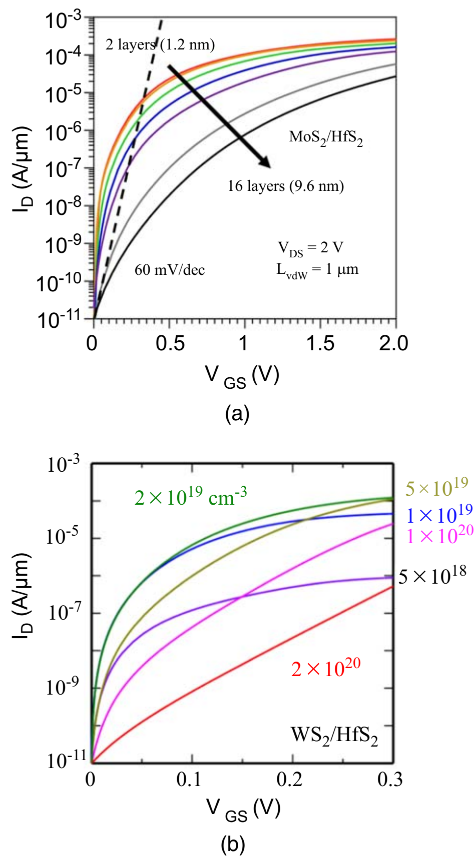

Fig. 8. (Color online) TCAD simulations of HfS_2-based vdW TFET using a non-local BTBT model. (a) Transfer characteristics dependence of HfS_2 channel thickness in MoS_2/HfS_2 vdW TFET. The length of the vdW heterojunction is 1 μm, the gate insulator is 5 nm HfO_2, the MoS_2 flake thickness is 10 nm, and the drain bias is 2 V. (b) Transfer characteristics dependence of source doping concentration in WS_2/HfS_2 vdW TFET. The length of the vdW heterojunction is 20 nm, the EOT of the gate insulator is 0.5 nm, the HfS_2 channel thickness is 1.2 nm (bilayer), the WS_2 source flake thickness is 3.6 nm (6 layers), and the drain bias is 0.3 V. The most appropriate doping level is around 2×10^{19} cm^{-3}.

SS of 300 mV dec^{-1}. Therefore, increasing the gate capacitance was manifested to be an effective solution to mitigate the impact of interface traps and improve the subthreshold slope in a vdW TFET.

According to Eq. (1), we estimated that the SS must be 67 mV dec^{-1} if the interface quality is ideal. We performed technology computer-aided design (TCAD) simulations of the HfS_2 thickness dependence of the MoS_2/HfS_2 vdW TFET based on the non-local BTBT model, and the results are shown in Fig. 8(a). The length of the vdW heterojunction was set to 1 μm, the gate insulator was 5 nm HfO_2, the MoS_2 flake thickness was 10 nm, and the drain bias was 2 V. The results indicated that when the HfS_2 channel exceeds 14 layers (8 nm), the SS degrades over 60 mV dec^{-1} because it is difficult to modulate the tunneling interface if the channel is thicker. The simulation results show a good fit to the evaluated experimental SS of 67 mV dec^{-1} because the HfS_2 flake thickness exceeded 10 nm. To obtain better performance, we calculated the *I–V* characteristics with another source material. Higher on-current could be estimated for a WS_2/HfS_2 vdW TFET. The dependence of SS on the source doping concentration in WS_2/HfS_2 vdW TFET is shown in Fig. 8(b). To boost the on-current, the length of the vdW heterojunction was set to 20 nm, the EOT of the gate insulator was 0.5 nm, the HfS_2 channel thickness was 1.2 nm, the WS_2 source flake thickness was 3.6 nm, and the drain bias was 0.3 V. We found that the extremely high doping level results in a restricted tunneling region, while a lower doping level leads to hole depletion, which increases the access resistance. The most appropriate doping level is around 2×10^{19} cm^{-3}, where a high on-current over 100 μA μm^{-1} could be achieved. Hence, further optimization of our p-MoS_2/HfS_2 vdW TFET towards sub-60 mV dec^{-1} operation should involve the reduction of the HfS_2 channel thickness to enhance the gate controllability. Also, doping technology in 2D materials should be improved for exact source doping concentrations. We believe that a good 2D channel-oxide interface combined with ultrathin channel thickness and well-designed doping concentration will pave the way to a high-performance vdW TFET.

4. Conclusions

In this report, we fabricated p-MoS_2/HfS_2 vdW TFETs and evaluated the properties of fabricated transistors. The different temperature dependence of both p-MoS_2/HfS_2 vdW TFET and HfS_2 MOSFET indicated that the turn-on current from p-MoS_2/HfS_2 vdW TFET was originated by BTBT. To suppress the gate leakage between S/D electrodes and back-gate, a buried Ni back-gate structure was introduced to reduce the overlapping area. The minimum SS was improved from 700 to 300 mV dec^{-1} when the EOT was reduced from 10.8 nm (25 nm Al_2O_3) to 3.7 nm (15 nm HfO_2), which manifested that increasing the gate capacitance was an effective solution to suppress the impact of interface traps in a vdW heterostructure TFET.

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