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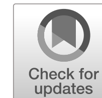

Enhanced bonding strength of InP/Si chip-on-wafer by plasma-activated bonding using stress-controlled interlayer

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To realize next-generation photonic integrated circuits based on the III–V/Si hybrid integration platform using chip-on-wafer (CoW) direct bonding technologies, high-yield collective bonding of InP chips on Si substrates with a high bonding strength is required. This study demonstrates high-yield InP/Si CoW plasma-activated bonding using a chip holder with pockets, the depth of which is precisely controlled. Additionally, finite element simulations are used to determine that the stress-controlled interlayer consisting of InP-based epitaxial layers with tensile strain effectively suppresses stress at the InP/Si bonding interface, which affects the bonding strength. Thus, a high bonding strength of 20 MPa in 2 mm × 2 mm InP chips on the Si substrate was achieved by introducing a superlattice structure consisting of GaInAsP and InP (with tensile strain) as the stress-controlled interlayer. © 2019 The Japan Society of Applied Physics

1. Introduction

The coherent transmission system using digital signal processing for multi-level modulation formats, such as quadrature phase-shift keying and quadrature amplitude modulation, has been widely applied to long-haul and metro-core networks, as it affords high receiver sensitivity and high resilience to linear impairments including chromatic dispersion and polarization mode dispersion.[1,2] Additionally, the adaption of the coherent transmission system has been promoted to the datacenter interconnect with the significant increase in its data traffic rate, accelerated by the expansion of cloud computing, social network services, and video streaming services.[3] This requires wide-bandwidth operation above 1 Tbps, low power consumption, miniaturization, and good cost effectiveness in terms of integrated photonic devices for coherent transmission. Although two major monolithic integration technologies based on InP and Si-on-insulator (SOI) have been developed, neither approach can simultaneously meet all requirements for coherent transmission systems for datacenter interconnects.

The Si photonics platform fabricated on a SOI substrate using a complementary metal–oxide–semiconductor-compatible process offers high-density integration on a large-diameter wafer and optical components with a small footprint owing to the large difference between the refractive indices of Si and SiO_2.[4,5] However, the monolithic integration of lasers on a Si photonics platform is very difficult because of the indirect bandgap of Si materials.

In contrast, InP-based monolithic integration technologies offer the monolithic integration of lasers as well as the wide-bandwidth operation and high efficiency of modulators and photodetectors.[6–8] However, InP-based photonic devices are not suitable for the miniaturization of devices and high-density integration on a large-diameter wafer. Therefore, a combination of appropriate devices for each section is desirable for the fabrication of next-generation photonic integrated circuits with good performance, miniaturization, and good cost effectiveness, utilizing the beneficial features of InP-based monolithic integration technologies and Si photonics; III–V/Si hybrid integration provides one such solution to address this issue.

Various approaches, such as the bonding of processed III–V chips,[9–11] transfer printing,[12,13] bonding using polymers,[14–16] and direct bonding,[17–21] have been studied for the realization of the III–V/Si hybrid integration platform. Direct bonding of a III–V wafer on a Si or SOI substrate has several advantages over other methods. Previously, high optical coupling efficiency between III–V active layers and Si waveguides[22] and electrical conductivity by III–V/Si interface[23] were indicated utilizing the advantage of features in this bonding approach. Additionally, the regrowth process of a device structure using a thin III–V layer bonded on a Si or SOI substrate by this approach has been presented.[24–26] A severe position alignment between III–V active layers and Si waveguides is not required in the bonding process because a device fabrication process using a conventional photolithography technique is implemented after the bonding, i.e. the position alignment is determined by photolithography.

Plasma-activated bonding (PAB), a direct bonding method, is the bonding process that utilizes relatively low temperature below 200 °C. Hence, it does not afford thermal effect which causes the degradation of III–V device properties. In previous studies, we reported the GaInAsP/SOI hybrid lasers fabricated via the wafer-to-wafer (WtW) bonding process using N_2-PAB.[27,28] High optical coupling efficiency between InP-based layers and Si-waveguides was also described through the double-taper-type coupler structures.[29,30] However, WtW PAB is not suitable for integrating various types of III–V epitaxial wafers with different designs. Further, the chip-on-wafer (CoW) bonding technique may be preferable[31] because it can reduce the III–V material waste, unlike the WtW bonding. For device fabrication using the InP/Si CoW bonding process, a high-yield and bonding strength above 15 MPa are necessary.[32]

This paper exhibits investigation results in the bonding strength of the InP/Si CoW bonding technique using InP-based epitaxial layers with strain introduced as a

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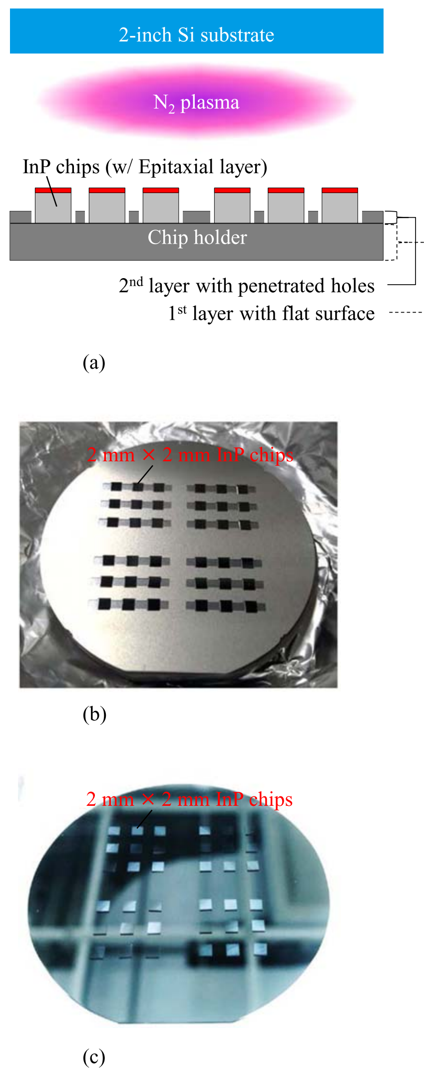

Fig. 1. (Color online) (a) Schematic diagram of CoW-PAB process, (b) photograph of the chip holder with InP chips and (c) photograph of InP/Si CoW.

stress-controlled interlayer. In addition to experimental results regarding the enhancement of bonding strength through the stress-controlled interlayer,[33] its effect on the suppression of vertical stress at the InP/Si bonding interface is described via theoretical analyzes.

2. InP/Si CoW bonding process

Figure 1(a) schematically shows the proposed InP/Si CoW-PAB process. Before the bonding process, a 2 inch InP wafer with epitaxial layers is diced into 2 mm square chips, and these chips are held onto a chip holder. Figure 1(b) shows the image of the chip holder with 36 InP chips. To accomplish the high-yield InP/Si CoW bonding process, the chip holder with pockets for holding InP chips was prepared, and the depth of the pockets was precisely controlled to uniformly align the height of chips on this holder, i.e. it was fabricated by bonding two plates with penetrated holes and flat surfaces. This approach offers a simpler bonding process compared with two-step bonding processes in which the temporal bonding of III–V chips on a carrier wafer using an adhesive layer is performed before the bonding of III–V chips on a Si wafer,[32] and no contamination is observed at the bonding interface originating from the adhesive material.[34] To avoid the degradation of the chip holder due to the plasma irradiation, this holder consists of a metal with a high melting point.

The typical bonding process is the following. In the vacuum chamber with the pressure of 10^{-4} Pa, N_2 plasma is irradiated onto the InP chips on the holder and a Si wafer. InP chips and Si wafer are bonded at a pressure of 4 MPa, and temperature of 150 °C. Figure 1(c) shows the image of the InP/Si CoW bonded via this process. Thirty-six InP chips were successfully bonded on a 2 inch Si wafer. The bonding strengths of these InP chips were evaluated by the die shear test, and a 10 MPa bonding strength was obtained as a median.[33,35]

3. Evaluation of bonding quality after InP substrate removal

Figure 2 shows the schematic of the cross-sectional image of the InP chip with epitaxial layers bonded on the Si wafer. The epitaxial layer was designed for the fabrication of active devices including GaInAsP multiple quantum wells, for an active layer with a peak wavelength of 1.55 μm. Additionally, it includes the superlattice layer consisting of 14 pairs of 7 nm thick GaInAsP and 6 nm thick InP as an interlayer for the suppression of damage due to the PAB process, which blocks the crystal defects linked to active layers caused by bonding process.[36] After the bonding of InP chips with epitaxial layers on the Si wafer, wet-chemical etching using a HCl solution was performed to remove the InP substrate. Figure 3 shows (a) the optical microscopy image of the surface of the InP chip and (b) the height mapping of the InP chip measured by a surface profiler after the removal of InP substrate. In region A at the center of the chip, the height of the chip is 2.9 μm, which is similar to the total thickness of epitaxial layers. This indicates that the InP chip is normally bonded on the Si wafer. In contrast, the height of the chip in region B is 0.3 μm greater than the total thickness of epitaxial layers, and the epitaxial layers are deduced to peel off from the Si wafer. Additionally, a chip height of 0.6 μm lower than the total thickness of epitaxial layers is observed in region C as the periphery of the chip. This indicates that a part of epitaxial layers disappears due to the side etching by the HCl solution.

Figure 4 shows the cross-sectional scanning electron microscopy (SEM) images of regions A–C. As in the case of chip height mapping, the normal bonding between the InP chip and epitaxial layers on the Si wafer is confirmed in

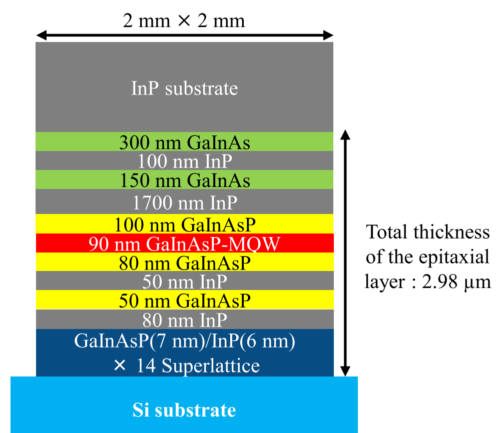

Fig. 2. (Color online) Schematic cross-sectional diagram of the InP chip with epitaxial layers bonded on the Si wafer.

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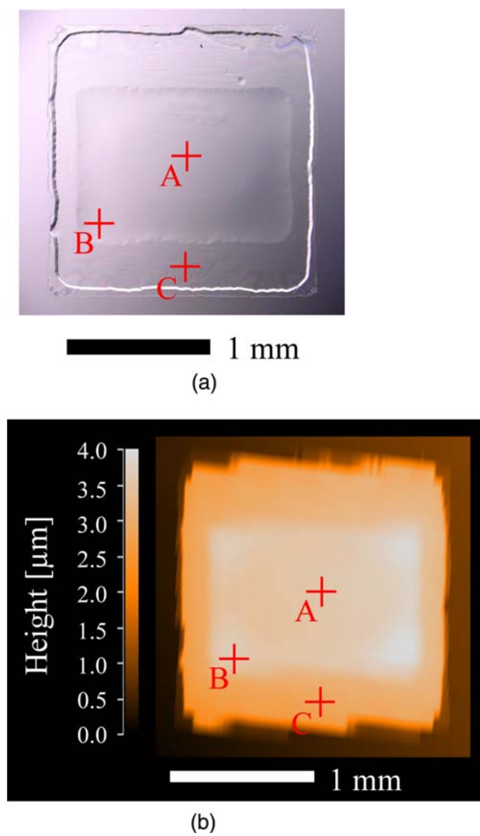

Fig. 3. (Color online) (a) Optical microscope image and (b) height mapping of the InP chip after substrate removal.

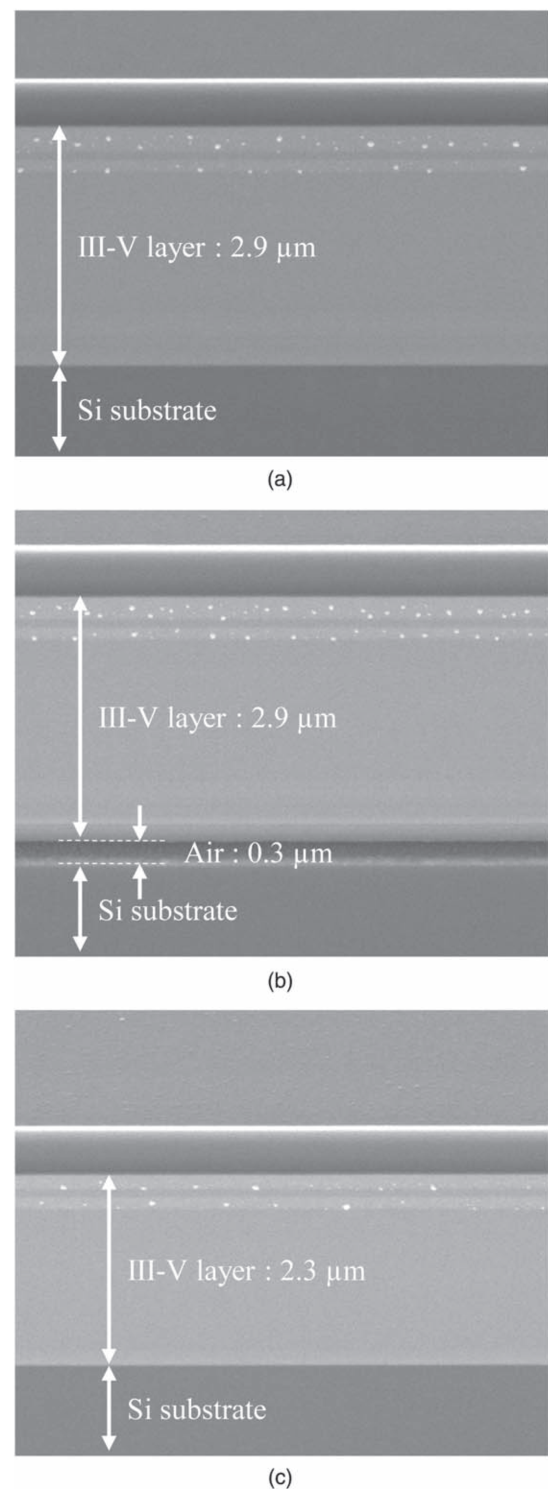

Fig. 4. Cross-sectional SEM images of region (a) A, (b) B, and (c) C for the InP/Si CoW bonding interface.

region A [Fig. 4(a)], and a void of 0.3 μm at the bonding interface is observed in region B [Fig. 4(b)]. Furthermore, the epitaxial layers in the vicinity of the bonding interface disappear in region C [Fig. 4(c)]. This is caused by the infiltration of the HCl solution into the bonding interface. Hence, the chip height estimation corresponds to the SEM images of bonding interfaces.

To estimate the bonding quality of the InP chip, photoluminescence (PL) was measured. Figure 5 shows (a) the PL intensity mapping at a wavelength of 1.55 μm and (b) PL spectra for the three regions of the InP chip shown in Fig. 3(a). 1064 nm yttrium–aluminum-garnet laser is used as the light source. Uniform PL intensity is observed in region A, the normally bonded area. In region B, the peeling off area, the PL intensity at 1.55 μm is higher than that in region A, and periodic intensity peaks are observed at 1.44 and 1.34 μm. These PL intensity peaks are attributed to the multi reflection by the void at the peeling off interface. Moreover, the PL intensity is negligible in region C, the side etching area. From these results, the evaluation method for determining the quality of the InP/Si CoW bonding interface through the measurement of chip height and PL intensity was established. In contrast, to avoid the peeling off of epitaxial layers and the side etching at the bonding interface, the improvement in bonding strength at the periphery of the InP/Si CoW interface was determined to be essential.

4. Numerical simulation of stress at the InP/Si CoW bonding interface

To investigate the poor bonding strength at the periphery of the InP chip, which was attributed to the stress at the InP/Si CoW bonding interface, a two-dimensional finite element method (2D-FEM) simulation was performed to determine the effect of stress at the bonding interface. Figure 6 shows the schematic for the calculation model. The calculation was performed in the area surrounded by a dashed line at the bonding interface of the 350 μm thick InP chip and a 550 μm thick Si substrate (Fig. 6). The material parameters listed in Table I were also used for this simulation. Using this model, the simulation was carried out for each step of the InP/Si CoW bonding process.

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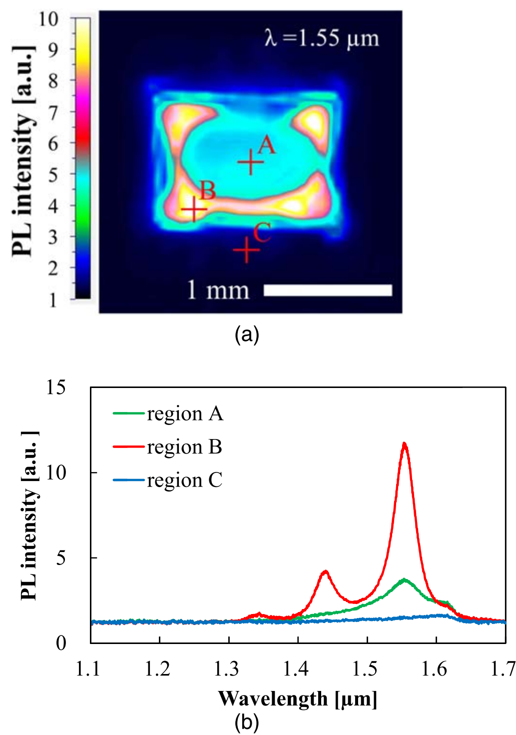

Fig. 5. (Color online) (a) PL intensity mapping and (b) PL spectra at region A, B, and C for the InP chip.

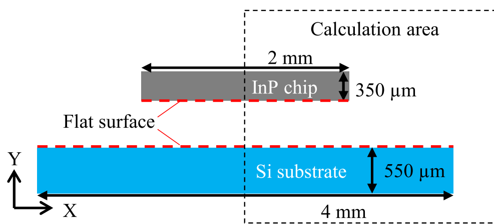

Fig. 6. (Color online) Schematic diagram of the InP/Si CoW bonding interface for 2D-FEM calculation.

Figure 7 shows the mapping of the calculated stress in the vertical direction for each bonding step at the edge of the InP/Si CoW bonding interface. In this simulation, it was assumed that the bonding pressure was uniformly applied at the bonding interface, and both surfaces of InP and Si were flat before the bonding. Before the bonding [Fig. 7(a)], the bonding surface of the InP chip was also assumed to be stress-free, i.e. epitaxial layers were not deposited on the InP chip. At the bonding step [Fig. 7(b)], the temperature was increased to 150 °C, and the InP chip was bonded onto the Si substrate with a pressure of 4 MPa. After bonding [Fig. 7(c)], the temperature was decreased to 25 °C. An extremely high tensile stress of above 100 MPa occurred at the edge of the InP/Si CoW bonding interface. This tensile stress was due to the larger thermal expansion coefficient of InP compared with that of Si, and it was considered that this stress affected the bonding strength at the edge of the InP/Si CoW bonding interface.

Additionally, a three-dimensional (3D)-FEM simulation was also performed to confirm the stress effect at the square corner of the InP/Si CoW bonding interface. Figure 8 shows the calculated vertical stress mapping after the bonding process through the 3D-FEM simulation. In similarity to the 2D-FEM simulation, high tensile stress was observed at the edge of the bonding interface, particularly at the square corner. Notably, the tensile stress in the 3D simulation was lower than that in the 2D simulation, because the mesh division of the adopted 3D simulation was rougher than that of the 2D simulation in terms of the calculation time. On the basis of these results, the suppression of high tensile stress at the edge of the bonding interface was determined to be indispensable for the improvement of bonding strength.

5. Introduction of stress control by strained interlayer

The stress control in the InP chip by the introduction of a strained interlayer was suggested to suppress the high tensile stress at the edge of the InP/Si CoW bonding interface. The 2D-FEM simulation (discussed in the previous section) was utilized for this investigation using the calculation model shown in Fig. 9(a). In this simulation, it was assumed that an InP-based interlayer with a strain of −0.3% (tensile strain) to +0.3% (compressive strain) and a thickness of 0.7 μm was formed on the bonding surface of an InP chip. Each strained interlayer results in the bowing of the InP chip. Figure 9(b) shows the calculated bowing profiles of InP chips with ±0.3% strained interlayers, before the bonding process. The interlayer with compressive strain affords a convex chip bowing, and the tensile strain affords a concave bowing.

Figure 10 shows the calculated vertical stress mapping at the edge of the InP/Si CoW bonding interface after the bonding process for (a) +0.3% compressive- and (b) −0.3% tensile-strained interlayers. In comparison to the result for the case without the strained interlayer shown in Fig. 7(c), the tensile stress at the edge of the bonding interface increases in the case of the compressive-strained interlayer, as shown in Fig. 10(a). Contrarily, tensile stress is well suppressed for the tensile-strained interlayer, as shown in Fig. 10(b). The maximum value of the calculated tensile stress in the vertical direction at the InP/Si bonding interface is plotted in Fig. 11 as dependence on the strain value of the interlayer. The interlayer with tensile strain results in a reduction of tensile stress at the bonding interface in comparison to that with compressive strain.

Figure 12 shows the schematic for the vertical stress at the InP/Si CoW bonding interface after the bonding process. As mentioned above, a high tensile stress existed at the edge of the bonding interface due to the larger thermal contraction of InP in comparison to that of Si. Even though the compressive-strained interlayer affords convex bowing to the InP chip before the bonding process, as shown in Fig. 9, it yields concave bowing in the bonding process, because the surface of the InP chip is flipped upside down in the bonding process,

Table I. Material parameters for 2D-FEM simulation.

	Young's modulus [GPa]	Poisson's ratio	Thermal expansion coefficient [ppm K^{-1}]	Density [g cm^{-3}]
InP	60.7	0.30	4.6	4.79
Si	130	0.27	2.6	2.33

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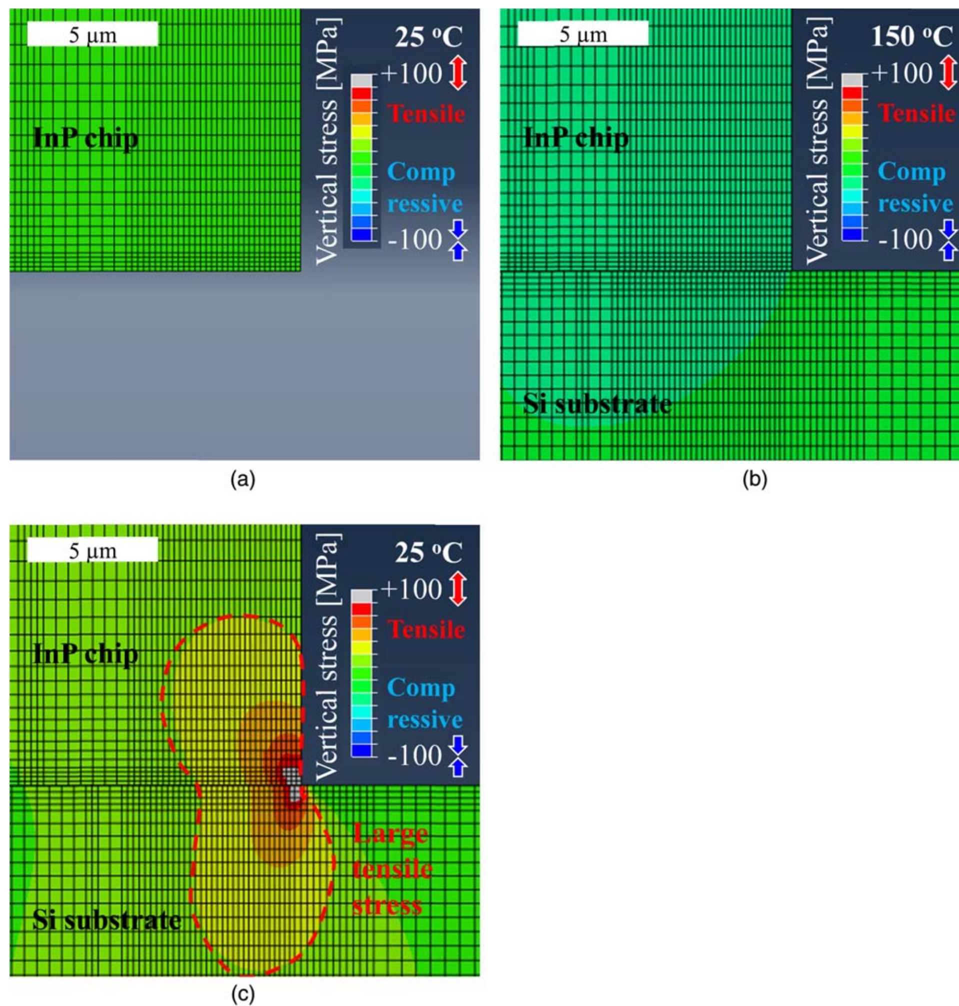

Fig. 7. (Color online) Vertical stress mapping calculated using 2D-FEM at the edge of the InP/Si CoW bonding interface (a) before the bonding, (b) at the bonding step and (c) after the bonding.

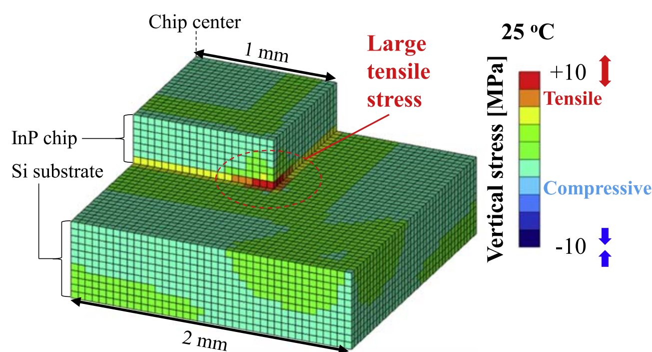

Fig. 8. (Color online) Vertical stress mapping calculated using 3D-FEM for the InP/Si CoW.

as shown in Fig. 12(a). Consequently, the tensile stress which induces a decline in bonding strength at the edge of the InP chip is enhanced due to the concave bowing after the bonding process. Similarly, although the tensile-strained interlayer affords concave bowing to the InP chip before the bonding process, as shown in Fig. 9(a), it yields convex bowing in the bonding process. Hence, the tensile-strained interlayer can compensate for the tensile stress due to thermal contraction at the edge of the InP/Si CoW bonding interface by convex bowing, which presses the edge of the InP chip on the Si substrate, as shown in Fig. 12(b). Accordingly, it was determined that the stress control of the InP chip by the strained interlayer was effective for the suppression of the tensile stress due to thermal contraction at the edge of the InP/Si bonding interface.

6. Experimental demonstration of stress-controlled interlayer

Introduction of the stress-controlled interlayer with strain for the improvement of the InP/Si CoW bonding strength was experimentally demonstrated using the wafer structure shown in Fig. 13. In order to remove the influence of strain effect on other layers, a simple wafer structure was adopted. This structure consisting of a GaInAs etching stop layer, an InP buffer layer, and a stress-controlled interlayer was prepared on a 2 inch InP wafer by organometallic vapor-phase epitaxial (OMVPE) growth. We have adopted the lattice-matched superlattice consisting of 14 pairs of 7 nm GaInAsP and 6 nm InP layers as an interlayer for the suppression of damage due to the PAB process. To make this superlattice structure function as the stress-controlled interlayer, the flow rate of the gallium precursor was varied, i.e. the composition of GaInAsP was changed to vary the strain values.

Figure 14 shows the X-ray diffraction $2\theta/\omega$ scan profiles of three wafers with different flow rates of the gallium precursor. As the flow rate of the gallium precursor increased, the first diffraction peak of the GaInAsP/InP superlattice

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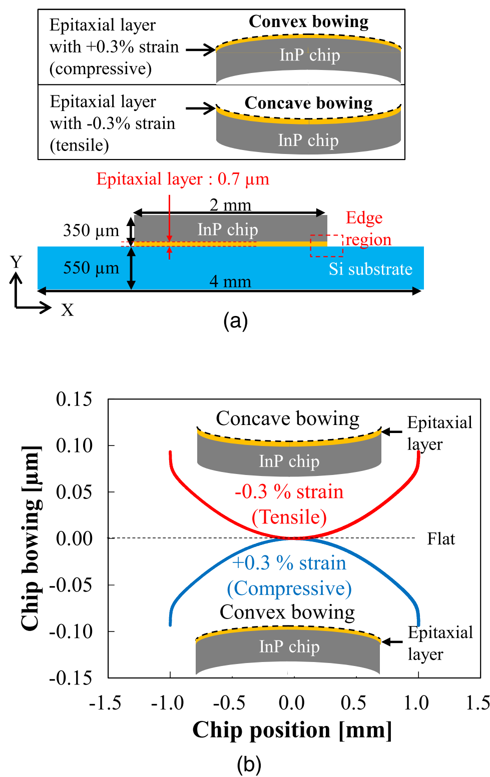

Fig. 9. (Color online) (a) Schematic diagram of the InP/Si CoW bonding interface with the strained interlayer for 2D-FEM calculation and (b) calculated bowing profiles of InP chips with the strained interlayer, which has +0.3% compressive strain or −0.3% tensile strain before the bonding process.

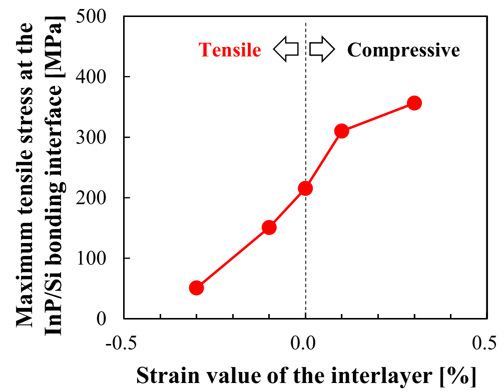

Fig. 11. (Color online) Dependence of the maximum value of calculated tensile stress toward vertical direction at the InP/Si bonding interface, on the strain value of the interlayer.

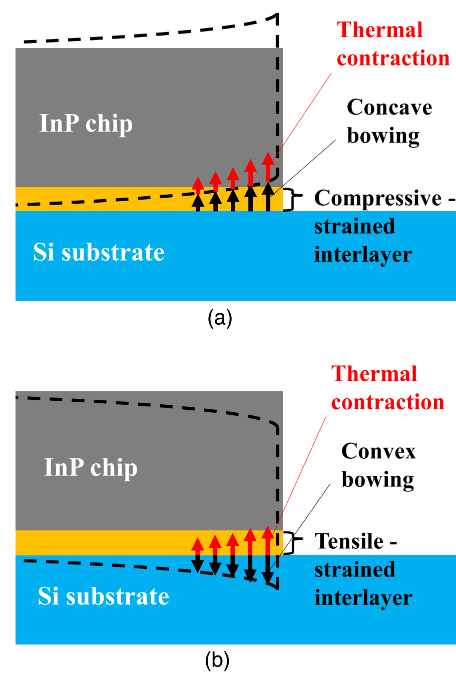

Fig. 12. (Color online) Schematic of the vertical stress at the InP/Si CoW bonding interface with (a) compressive-strained interlayer and (b) tensile-strained interlayer.

layer shifted to a wider angle, and the composition of GaInAsP was changed to generate tensile strain. As a result, the three prepared wafers exhibited +0.02% nearly lattice matching, −0.18% tensile strain, and −0.28% tensile strain ($\Delta a/a$), respectively.

The extent of wafer-bowing was measured using a surface profiler for these three wafers, before and after OMVPE growth. Then, the change in the extent of wafer-bowing was estimated, as shown in Fig. 15. As can be seen, the wafer-bowing shifted from convex to concave, as the superlattice layer has relatively larger tensile strain. The wafer stress σ as

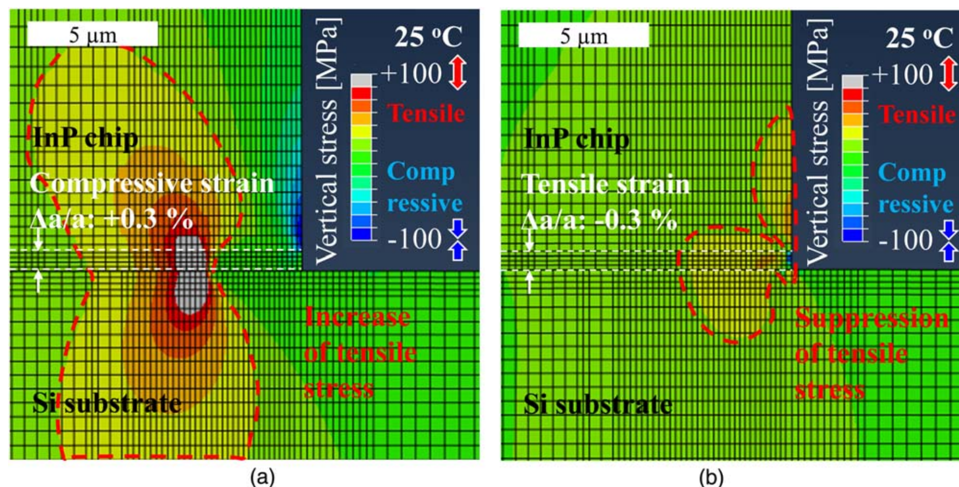

Fig. 10. (Color online) Vertical stress mapping calculated using 2D-FEM at the edge of the InP/Si CoW bonding interface in the case of (a) +0.3% compressive-strained and (b) −0.3% tensile-strained interlayers.

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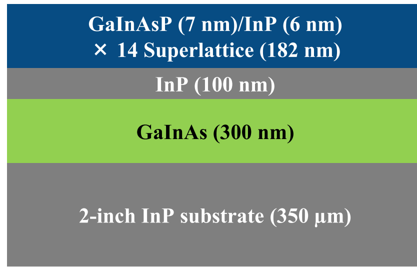

Fig. 13. (Color online) Wafer structure for experimental demonstration of the stress-controlled interlayer having InP-based epitaxial layers with strain.

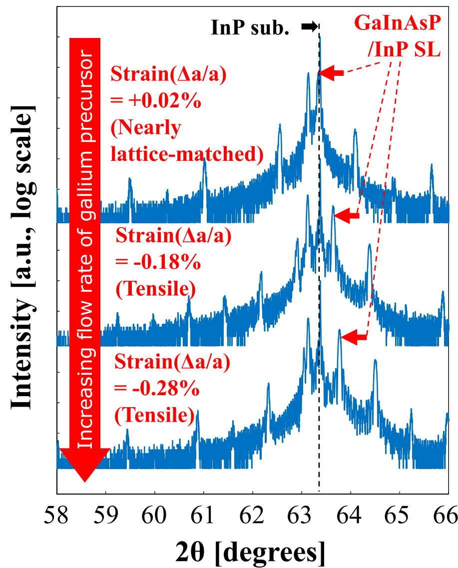

Fig. 14. (Color online) XRD 2θ/ω scan profiles of epitaxial wafers with the stress-controlled interlayer consisting of the strained GaInAsP/InP superlattice structure.

a function of the position on the wafer, x, was calculated from these wafer-bowing profiles using Stoney's equation given by[37,38])

$$\sigma(x) = \frac{1}{6K(x)} \cdot \frac{E}{(1-\nu)} \cdot \frac{t_s^2}{t_f}, \quad (1)$$

where E, ν, t_s, and t_f represent the Young's Modulus, the Poisson's Ratio, the thickness of an InP wafer, and the thickness of an epitaxial layer, respectively. $K(x)$ represents the change in the radius of the bowing curvature, as given by

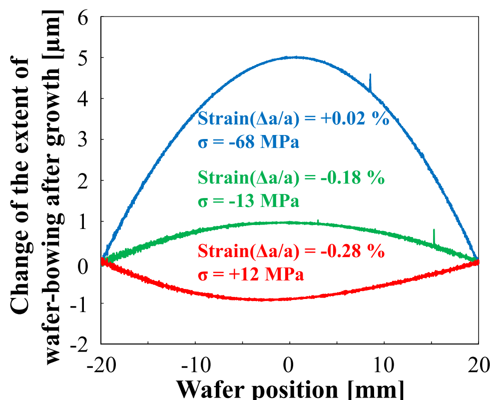

Fig. 15. (Color online) Wafer-bowing profiles of epitaxial wafers with different strain as the stress-controlled interlayer.

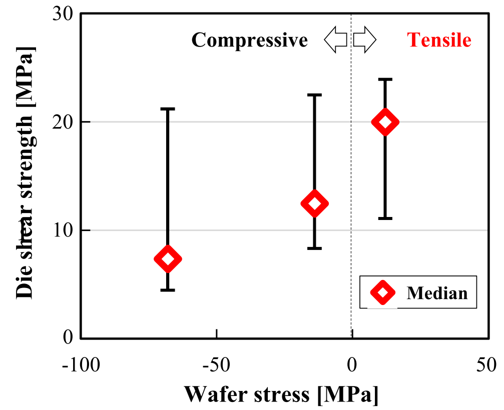

Fig. 16. (Color online) Dependence of die shear strength on wafer stress by stress-controlled layers with compressive and tensile strain.

$$\frac{1}{K(x)} = \frac{1}{R_f(x)} - \frac{1}{R_s(x)}, \quad (2)$$

where $R_f(x)$ and $R_s(x)$ represent the radius of the bowing curvature for an InP wafer before and after OMVPE growth, respectively. Stress-controlled layers with +0.02% nearly lattice matching, −0.18% tensile strain, and −0.28% tensile strain had a compressive wafer stress of −68 MPa, compressive wafer stress of −13 MPa, and tensile wafer stress of 12 MPa as an average value for the entire InP wafer, respectively. Hence, we obtained tensile wafer stress accompanied by concave bowing with the stress-controlled layer having −0.28% tensile strain, which is necessary to suppress the tensile stress at the edge of the InP/Si CoW bonding interface. Eventually, this yields convex bowing in the bonding process, in which the surface of InP chips is flipped over, as indicated in Sect. 5.

These wafers were diced to 2 mm square chips and bonded on the Si wafer to estimate the InP/Si CoW bonding strength. Figure 16 shows the dependence of die shear strength on wafer stress for the three wafers. Since it was difficult to estimate the stress of small InP chips, we assumed that the chip stress was almost the same as the wafer stress before dicing. As can be seen, compared with compressive wafer stress, tensile wafer stress resulted in a larger bonding strength. Die shear strength of 20 MPa was acquired as a median value for InP chips with a tensile wafer stress of 12 MPa. Thus, we experimentally demonstrated the enhancement of bonding strength through the stress-controlled interlayer with tensile strain, as predicted by FEM simulation.

7. Conclusions

We demonstrated the direct bonding of InP chips on Si wafer by PAB using the proposed chip holder and the stress-controlled interlayer consisting of a strained GaInAsP/InP superlattice structure. To suppress the peeling off of InP-based layers and the extensive side etching after removal of the InP substrate by wet-chemical etching, improvement of bonding strength at the edge of the InP/Si bonding interface through the compensation of thermal contraction by using the stress-controlled interlayer was investigated by FEM simulation; enhancement of bonding strength by the tensile-strained interlayer was anticipated. The superlattice structure consisting of GaInAsP and InP was introduced as the stress-controlled

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interlayer with tensile strain. A high bonding strength of 20 MPa was successfully achieved with the −0.28% tensile-strained interlayer. Therefore, we demonstrated that stress control with the strained interlayer introduced in the InP chip is very effective for the realization of high-yield InP chips on Si wafer using PAB processes, which will facilitate the development of next-generation photonic integrated circuits and could be applicable to other bonding methods.

Acknowledgments

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