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# Wafer and chip-level characterization of edge-coupled photonic integrated circuits by cascaded grating couplers and spot-size converters

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This study presents an efficient testing process for characterizing silicon photonic ICs. This process utilizes a coupling structure that integrates grating couplers and spot-size converters for efficient testing both at the chip and wafer levels, respectively. By leveraging wafer-level testing to estimate the characteristics of final chip-level devices, we anticipate a reduction in testing costs. To demonstrate the validity of the proposed testing process, we fabricated and measured silicon-on-insulator ring resonator devices on both wafer and chip levels. The results showed good agreement between the two levels of measurement, validating the effectiveness of our proposed testing process.


In recent years, the fabrication of silicon photonic ICs (Si PICs) using CMOS-compatible processes has enabled the development of cost-effective silicon chips with both optical and electrical functionalities.[1–5] This technology serves as a high-performance platform for photonics–electronics convergence, offering promising applications across various industries.[6–9] To enhance the integration and functional density of silicon photonics, heterogeneous and hybrid integration methods have been proposed to combine various material systems with diverse optical functionalities within a single package.[10,11] However, the overall cost of PIC-based modules is significantly influenced by testing, assembly, and packaging processes, which can account for approximately 80% of the total cost of conventional InP PIC-based modules.[12,13] Product testing alone contributes up to approximately 29% of the total cost,[14] a figure that can increase to approximately 60%–90% for less developed silicon photonics technology.[15] Therefore, reducing testing, assembly, and packaging costs is crucial for decreasing the overall cost of Si PIC-based modules.

Previous studies have employed two major strategies to reduce testing costs: utilization of enhanced testing structures,[16] and enhancing the automation level of the testing process.[14] In PICs, a prevalent testing method involves signal tapping through directional couplers with unbalanced splitting ratios, such as 99:1. This configuration allows 99% of the signal to pass through the waveguide normally, whereas 1% is tapped off to the testing branch.[17] The tapped-off signal is typically coupled to the testing equipment through surface couplers, facilitating the utilization of automatic wafer-level testing systems for in situ and screening tests.[18] However, surface grating couplers (GCs) encounter limitations in terms of bandwidth, polarization, and efficiency during the assembly and packaging phases.[19] In contrast, edge coupling utilizing spot-size converters (SSCs) offers advantages, such as increased bandwidth, reduced polarization sensitivity, and enhanced coupling efficiency.[20] However, edge coupling presents challenges, such as larger footprints associated with SSCs, fixed coupling positions, limited alignment tolerance, and stringent specifications at the coupling facet.[21]

To leverage the benefits of both methods, Novack et al. proposed a system that utilizes surface and edge coupling for efficient testing and packaging, respectively.[22] In this system, the signal is tapped through a GC after traversing two consecutive back-to-back SSCs. During testing, both SSCs exhibit optical transparency owing to their broadband characteristics and minimal optical loss. Subsequently, in the assembly and packaging phases, the chip is cleaved between both SSCs to enable edge coupling with external fibers or other chip dies. Conventionally, only specific test element groups are measured by surface coupling, with no other devices being measured until chip cleavage. After chip cleavage, final tests were conducted on all the device chips by edge coupling. Although this approach focuses on the overall process yield, it may result in unnecessary costs as the final tests include devices that could have failed in previous process steps.

This study proposes a testing process that utilizes a cascaded GC and SSC coupling structure to perform in situ and screening tests for all devices at the wafer level while performing final device tests, particularly for functional devices at the chip level. By detecting and eliminating failed chips through robust wafer-level tests the time-consuming chip-level tests can be reduced. Additionally, we validated the proposed testing process on a silicon-on-insulator (SOI) platform by comparing the device characterization results of ring resonator (RR) devices at both wafer and chip levels.

An example of the proposed testing process flowchart at the wafer and chip levels using surface and edge coupling, respectively, is shown in Fig. 1(a). A wafer-level testing system with an automatic wafer prober was employed for in situ testing during the fabrication process, as well as screening tests,[18] similar to the low-cost vertical-cavity surface-emitting laser fabrication process. Following these tests, the devices were cleaved to the die form for final product tests at the chip or package level. The primary advantage of our proposed process is the elimination of known-bad-die (failed devices in the wafer-level test), ensuring that only known-good-die are considered subsequently. Additionally, if certain characteristics are expected to be consistent at both the wafer and chip levels, those characteristics can be measured once during wafer-level tests and omitted during chip-level tests.

The schematic of the proposed wafer layout of a Si PIC (e.g., a silicon photonic transceiver)[23] with cascaded GC and SSCs coupling structures is shown in Fig. 1(b). The wafer was divided into a 2D array of chips, each typically equipped

 

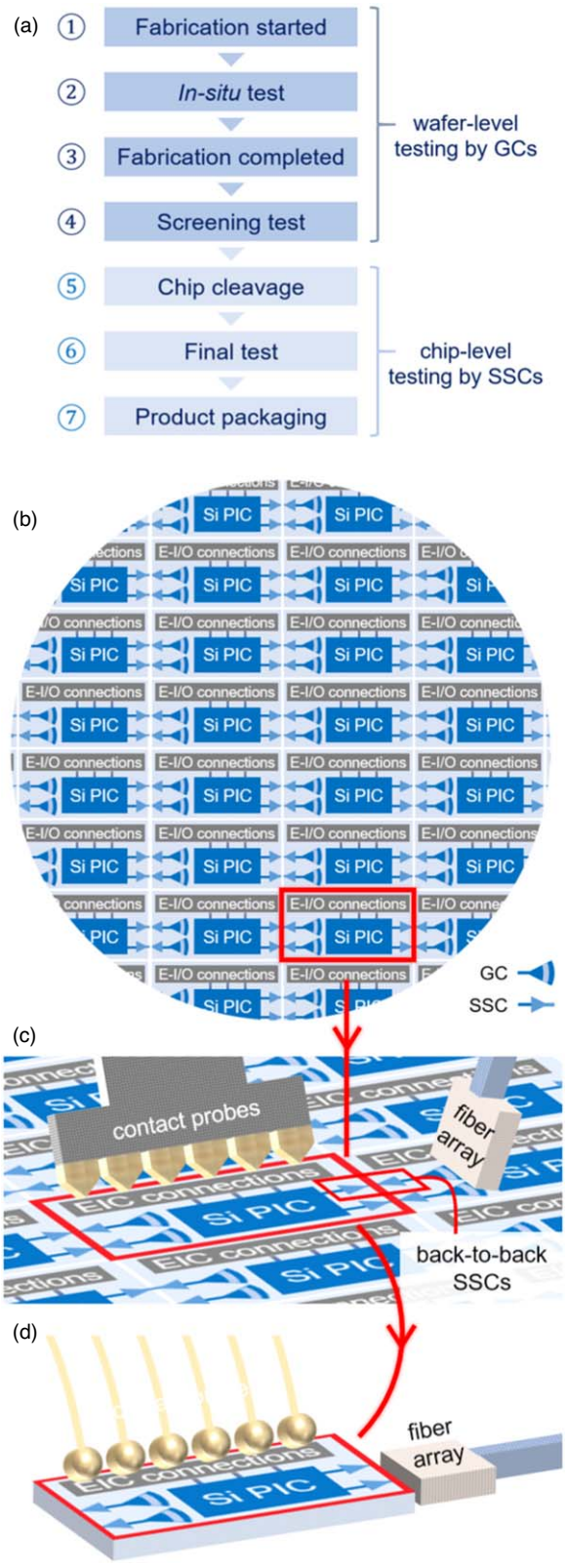


**Fig. 1.** Schematics of Si PIC illustrating the proposed (a) process flow, (b) wafer layout with cascaded GC and SSCs coupling structures, (c) in situ and screening tests conducted through surface coupling, and (d) final tests performed by edge coupling.

with electrical input/output (E-I/O) connections. However, the GC connected to each chip for surface coupling was located in the adjacent chip for space conservation. Additionally, back-to-back SSCs were aligned with the chip dicing planes to enable high-efficiency edge coupling after cleavage. A schematic of in situ and screening tests performed at the wafer level by surface coupling to a fiber array with E-I/O probes in contact is shown in Fig. 1(c). After cleavage, the functional devices underwent final device testing, followed by assembly and packaging. A schematic of the final device testing performed at the chip level by edge coupling to optical fiber arrays with connected E-I/O bonding wires is shown in Fig. 1(d).

To validate the proposed testing process, RR devices were fabricated on an SOI platform with cascaded GC and SSCs coupling structures connected to all the device ports. Subsequently, the devices were measured using surface and edge coupling at the wafer and chip levels, respectively. If these two characteristics, excluding coupling efficiency, are aligned, the validity of the proposed process can be established. The schematic of the fabricated Si PIC design is shown in Fig. 2. Notably, the GCs and SSCs can be arranged in arrays to decrease the testing time if the measurement permits. In this demonstration, the design featured a $1 \times 12$ array of focusing GCs that aligned with the fiber array of our automated wafer probing system. The period and duty cycle of the GC corrugations were 760 nm and 50%, respectively. The GC array was connected to eight SSCs (four on each facet) for chip-level measurements using two lensed fibers. The SSCs were introduced by tapering the single-mode SOI waveguides from 0.5 to 0.2 $\mu$m over a taper length of 100 $\mu$m. Both SSCs were connected back-to-back by a 200 $\mu$m long waveguide section with 0.2 $\mu$m width for mode matching with the lensed fibers. The expected loss introduced by this section is $<$0.1 dB. The Si PIC was fabricated on an SOI wafer with a top Si layer thickness of 220 nm using electron-beam lithography. The patterns were formed with a single etching step at a depth of 190 nm using inductively coupled plasma reactive ion etching. Finally, the wafer was cladded with $SiO_2$ with a thickness of approximately 1 $\mu$m by plasma-enhanced chemical vapor deposition.[24)]

Figure 3 shows Schematic view of surface and edge coupling for wafer and chip level testing with GCs and SSCs, respectively. The wafer-level test of the fabricated Si PIC using the automated wafer probing system (Formfactor CM300ph).[25)] The setup included a tunable laser source with a polarization synthesizer for light input, an optical power meter at the output, and a matrix switch that connected both the input and output to the fiber array. The testing was performed at an incident angle of 10°, fiber distance of 100 $\mu$m, and alignment wavelength of 1550 nm. The measured propagation loss at this wavelength was approximately 1.9 dB cm$^{-1}$. After cleavage, chip-level testing was conducted by edge coupling setup. In this setup, testing was performed by manually aligning the lensed fibers with the SSCs.

The measurements were conducted across the C-band for telecommunication applications. For wafer-level measurements, a tunable laser source was utilized to scan the wavelengths while monitoring the received power at each port using a power meter. However, in chip-level measurements, wideband amplified spontaneous emission light was introduced and the transmitted light was measured using an optical spectrum analyzer. Through both testing configurations, the stage temperatures were rigorously maintained at

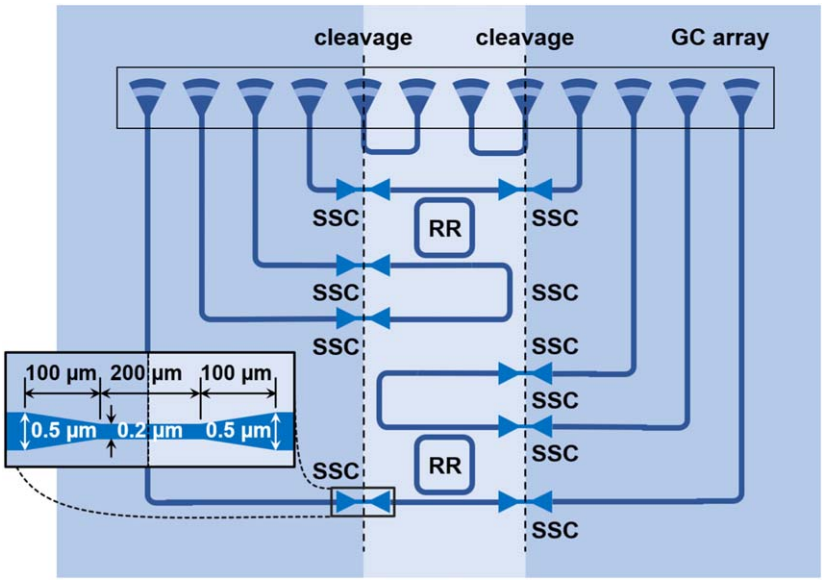


**Fig. 2.** Schematic of the coupling structure on an SOI with RR devices under test. Inset: two back-to-back SSCs connected by narrow a waveguide by which the dicing line passes.

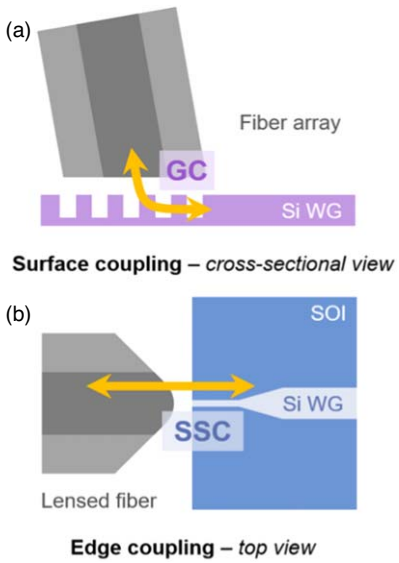


**Fig. 3.** Schematic view of (a) surface and (b) edge coupling for wafer and chip level testing with GCs and SSCs, respectively.

25 °C, and wavelength resolutions were uniformly set to 0.02 nm to ensure that the RR spectral shift and extinction ratio were not influenced differently by the test setups. The transmission spectra of the through and drop ports of the RR device measured at the wafer and chip levels by surface and edge coupling, respectively, are shown in Fig. 4. In both measurements, the coupling losses were derived from the reference waveguides and subsequently subtracted from the measured transmission spectra for normalization.

The results indicated a strong correlation between both wafer and chip-level measurements, underscoring the validity of the proposed testing process on the SOI platform. The utilization of wafer-level testing proved instrumental in accurately estimating the characteristics of the final chip-level devices. Additionally, spectral ripples were observed, owing to minor reflections within the testing circuit. The free spectral range of these ripples, shown in the insets of Fig. 4(b), aligned with the Fabry–Pérot cavities formed by reflections at the input and output coupling structures. That is, GC-to-GC and facet-to-facet reflections were utilized for the wafer- and chip-level measurements, respectively. The extracted ripple amplitudes corresponded to effective reflectivities of 8% and 14% for surface and edge coupling, respectively. These ripples were anticipated to be mitigated by utilizing GCs with low backscattering,[26] and cleaved facets with antireflection coatings.[27] It should be noted that dicing saw was used in this work for proof of concept. Thus, other cutting methods can be used as well. However, position tolerance should be taken into account for any cutting method. The 0.2 $\mu$m waveguide section between SSCs should be long enough to cover these tolerances. As dicing saws typically have larger tolerance $\sim$10 $\mu$m, and the cutting line does not need to be exactly in the center, a length of few tens of microns is actually enough to guarantee that the cutting line does not pass by SSC tapers. However, a length of 200 $\mu$m was used here for relaxed alignment constraints.

In summary, this study proposed and implemented an efficient testing process for the characterization of Si PICs. The process leveraged cascaded GC and SSCs as coupling structures, allowing for both surface and edge coupling during wafer- and chip-level testing, respectively. At the wafer level, in situ and screening tests were performed on all devices. Following chip dicing, final device tests were performed at the chip level, focusing on the functional devices. Thus, time-consuming chip-level tests were reduced by detecting and eliminating all the failed chips using robust wafer-level testing. The proposed testing process was validated using Si PICs comprising RR devices with cascaded GC and SSCs connected to all device ports. The good agreement between the device characterization results obtained at both the wafer and chip levels demonstrated the effectiveness of wafer-level testing in estimating the characteristics of the final chip-level devices.

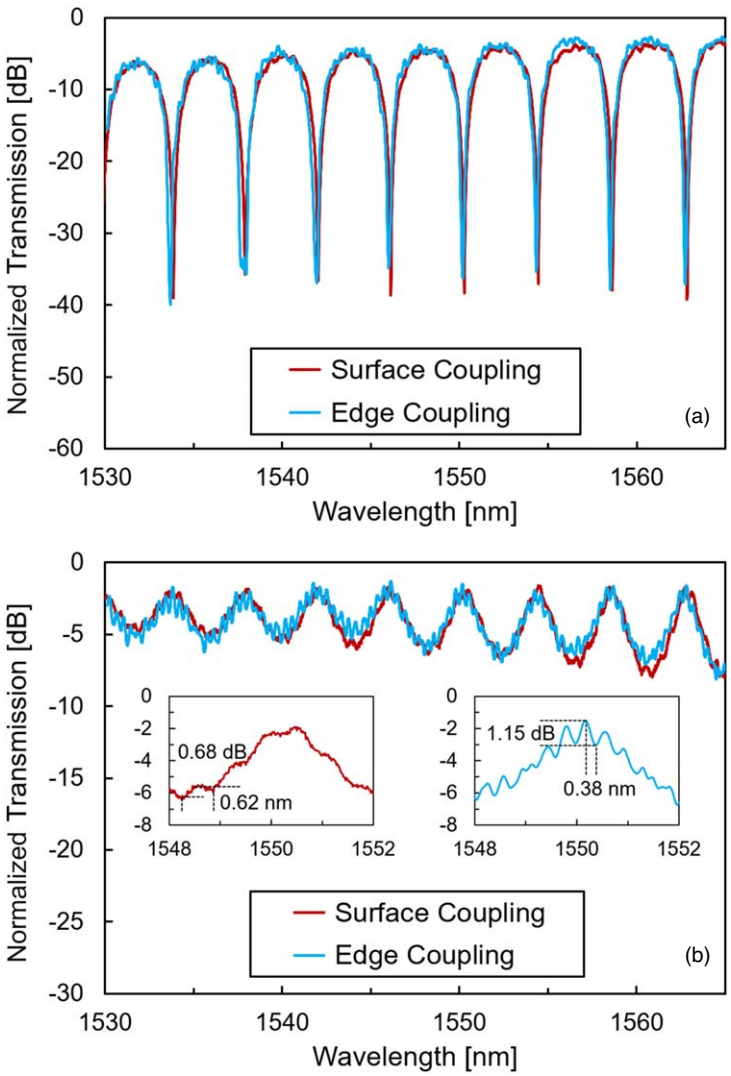


**Fig. 4.** Normalized transmission spectra of (a) through, and (b) drop ports of an RR device measured using surface and edge coupling. Inset: signal ripple amplitude and FSR for characterization of back-reflection.

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1) K. Schuster, S. Unger, C. Aichele, F. Lindner, S. Grimm, D. Litzkendorf, J. Kobelke, J. Bierlich, K. Wondraczek, and H. Bartelt, Adv. Opt. Techn. **3**, 447 (2014).
2) L. Carroll et al., Appl. Sci. **6**, 426 (2016).
3) S. R. Forrest, Proc. IEEE **75**, 1488 (1987).
4) R. A. Soref, Proc. IEEE **81**, 1687 (1993).
5) L. C. Kimerling et al., Proc. SPIE **6125**, 612502 (2006).
6) N. Margalit, C. Xiang, S. M. Bowers, A. Bjorlin, R. Blum, and J. E. Bowers, Appl. Phys. Lett. **118**, 220501 (2021).
7) C. Rogers et al., Nature **590**, 256 (2021).
8) J. Xie, W. Ye, L. Zhou, X. Guo, X. Zang, L. Chen, and Y. Zhu, J. Nanomater. **11**, 1646 (2021).
9) M. F. Gonzalez-Zalba, S. D. Franceschi, E. Charbon, T. Meunier, M. Vinet, and A. S. Dzurak, Nat. Electron. **4**, 872 (2021).
10) R. Baets and A. Rahim, Opt. Mater. Express **13**, 3439 (2023).
11) P. Kaur, A. Boes, G. Ren, T. G. Nguyen, G. Roelkens, and A. Mitchell, APL Photonics **6**, 061102 (2021).
12) SMART Photonics (www.smartphotonics.nl) (June 30th, 2022), Silicon photonics and indium phosphide: brother and sister.
13) JePPIX roadmap 2018 The road to a mulit-billion Euro market in integrated photonics, 2018, (www.jeppix.eu).
14) S. Latkowski, D. Pustakhod, M. Chatzimichailidis, W. Yao, and X. J.-M. Leijtens, IEEE J. Sel. Top. Quantum Electron. **25**, 1 (2019).
15) K. Heyman, Standards: The next step for silicon photonics (www.semi-engineering.com) (March 7th, 2023).
16) R. Polster, L. Y. Dai, M. Oikonomou, Q. Cheng, S. Rumley, and K. Bergman, Proc. SPIE **10537**, 1053703 (2018).
17) M. M. Osman, M. Chagnon, X. Xu, Q. Zhuge, M. Poulin, Y. Painchaud, M. Pelletier, C. Paquet, and D. V. Plant, Opt. Express **22**, 5693 (2014).
18) T. Horikawa et al., IEEE J. Sel. Top. Quantum Electron. **24**, 1 (2018).
19) D. Taillaert, W. Bogaerts, P. Bienstman, T. F. Krauss, P. Van Daele, I. Moerman, S. Verstuyft, K. De Mesel, and R. Baets, IEEE J. Quantum Electron. **38**, 949 (2002).
20) V. R. Almeida, R. R. Panepucci, and M. Lipson, Opt. Lett. **28**, 1302 (2003).
21) X. Mu, S. Wu, L. Cheng, and H. Y. Fu, Appl. Sci. **10**, 1538 (2020).
22) A. Novack, M. A. Streshinsky, and M. J. Hochberg, US Patent 10,359,567 (2019).
23) S. Y. Siew et al., J. Light. Technol. **39**, 4374 (2021).
24) M. Eissa, T. Mitarai, T. Amemiya, Y. Miyamoto, and N. Nishiyama, Jpn. J. Appl. Phys. **59**, 126502 (2020).
25) E. J. Marinissen, B. D. Wachter, T. Wang, J. Fiedler, J. Kiesewetter, and K. Stoll, IEEE Int. Test Conf. ITC2015, 10.1109/TEST.2015.7342412.
26) Y. Wang, X. Wang, J. Flueckiger, H. Yun, W. Shi, R. Bojko, N. A.-F. Jaeger, and L. Chrostowski, Opt. Express **22**, 20652 (2014).
27) S. Chattopadhyay, Y. F. Huang, Y. J. Jen, A. Ganguly, K. H. Chen, and L. C. Chen, Mater. Sci. Eng. **69**, 1 (2010).