

# **High-temperature and high-efficiency operation of a membrane optical link with a buried-ridge-waveguide bonded on a Si substrate**

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**Abstract:** We demonstrate a membrane photonic integrated circuit (MPIC) that includes a membrane distributed feedback (DFB) laser and a p-i-n photodiode with a buried-ridge-waveguide (BRW) on a Si substrate, using a-Si nanofilm-assisted room-temperature surface activated bonding (SAB) for on-chip optical interconnection. The BRW structure enhanced the lateral optical confinement compared with that of the conventional flat structure. The directly bonded membrane DFB laser using SAB had a lower thermal resistance and higher output power than the previous structure using a benzocyclobutene (BCB) bonding layer. The DFB laser had a low threshold current of 0.27 mA at 25 °C. The maximum detected photocurrent and slope efficiency were 0.95 mA and 0.203 mA/mA, respectively, at 25 °C. The MPIC was successfully operated at temperatures up to 120 °C. The 3-dB bandwidths of 16.8 GHz and 10.1 GHz were achieved at 25 °C and 80 °C, respectively, and 25 Gbps and 15 Gbps non-return-to-zero (NRZ)  $2^{15}$ -1 pseudo-random bit sequence signals were recorded at 25 °C and 80 °C, respectively.

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# **1. Introduction**

The scaling down of transistors is an important factor in improving the performance of large-scale integrated circuits (LSI). However, some drawbacks exist in the interconnection for connecting transistors. As the complexity of the interconnect increases, greater Joule heating and RC delay become impossible to ignore, especially in copper global wiring (to connect relatively long distance transistors to transistors, blocks to blocks). Novel on-chip electrical interconnection methods have been proposed to address this problem. Inductive coupling uses near-field coupling in a three-dimensional system integration structure between on-chip coils. Low power consumption of 10 fJ/bit at 1.1 Gbps was achieved [\[1\]](#page-7-0). However, the link distance was limited to a short region between the contacted chips. Another method is an on-chip transmission line interconnect that treats transmission signals on semiconductor chips as electromagnetic waves [\[2,](#page-7-1)[3\]](#page-7-2). This method has low latency, low power consumption, and low crosstalk compared to the conventional RC wiring. However, the size is large (several millimeters) and the two lines should be uniform. On-chip optical interconnection is attracting attention as a method for solving the interconnection bottleneck of LSI and many low-power-consumption light sources have been demonstrated, such as vertical-cavity surface-emitting lasers (VCSELs) [\[4](#page-7-3)[,5\]](#page-7-4) and photonic crystal (PhC) lasers [\[6](#page-7-5)[,7\]](#page-7-6). To integrate lasers on an LSI with an in-plane structure, the VCSELs should be combined with a 45° reflection mirror [\[8\]](#page-7-7). Optical links using PhC lasers, photonic crystal

waveguides, and p-i-n photodiodes (PD) have been demonstrated. The PhC laser showed a low threshold current of 22 µA, and an energy cost of 28.5 fJ/bit at 4 Gbps [\[9\]](#page-7-8). The bit error rate and larger data transmission were not evaluated because of the small output power of the PhC laser and the small bandwidth of the PD.

The concept of a membrane structure-based photonic integrated circuit (MPIC) has been proposed for on-chip optical interconnection on Si substrates obtained by benzocyclobutene (BCB) bonding [\[10\]](#page-7-9). The membrane structure uses a thin semiconductor core layer sandwiched between a material of low refractive index, such as air, and  $SiO<sub>2</sub>$  as the cladding layer for high optical confinement. Hence, an ultra-low threshold operation of the membrane laser can be realized, and a high speed can be obtained with a small-sized membrane PD. In our previous work, a membrane distributed-reflector (DR) laser with a high speed of 20 Gbps and low power consumption of 93 fJ/bit was demonstrated [\[11\]](#page-7-10). A membrane p-i-n PD was designed [\[12](#page-7-11)[,13\]](#page-7-12), and a high-speed of 20 Gbps GaInAs-bulk membrane p-i-n PD was achieved [\[14\]](#page-7-13). Another group also demonstrated a membrane laser of high 3-dB modulation bandwidth of 108 GHz on a silicon carbide substrate [\[15\]](#page-8-0). For the membrane optical link, integration was performed using a butt-jointed built-in (BJB) integrated membrane distributed-feedback (DFB) laser, passive GaInAsP waveguide, and membrane p-i-n PD at room-temperature [\[16,](#page-8-1)[17\]](#page-8-2). However, the large thermal resistance limited the output power of the membrane DFB laser and high-temperature operation was not investigated. Here, we report the high-temperature operation of an MPIC with a buried-ridge-waveguide (BRW) [\[18\]](#page-8-3) on Si bonded by a-Si assisted room-temperature surface-activated bonding (SAB) [\[19](#page-8-4)[,20\]](#page-8-5). For the static characteristics, laser injection current versus detected photocurrent was measured for temperature  $>100$  °C, and lasing operation was achieved at 120 °C. In terms of dynamic characteristics, small and large signal modulation were measured for 25-80 °C.

# **2. Device structure and fabrication**

The schematic of the membrane optical integrated circuit was shown in Fig. [1\(](#page-2-0)a). This membrane optical link consists of a membrane DFB laser of 70 µm length, passive GaInAsP waveguide of 500 µm length, and p-i-n membrane PD of 200 µm length. The stripe width and distance between  $p$ -electrode and active region were 1.0  $\mu$ m and 1.7  $\mu$ m, respectively, in design. The waveguide has the same width with laser. Figure [2](#page-2-1) illustrates the fabrication process of MPIC. The initial epitaxial wafer consisted of a 267 nm thick core layer including a GaInAsP five-quantum-well active layer with a photoluminescence peak wavelength of 1549 nm sandwiched between GaInAsP optical confinement layers, a *p* + -GaInAs contact layer, and InP/GaInAs etch-stop layers grown by organometallic vapor-phase-epitaxy (OMVPE). The device fabrication started with three-steps OMVPE selective area regrowth to form a passive waveguide,  $n$ -InP ( $N_D = 2 \times 10^{18}$ /cm<sup>3</sup>) and  $p$ -InP ( $N_A = 5 \times 10^{17}$ /cm<sup>3</sup>) side cladding layers. By controlling the growth time of selective area regrowth in the OMVPE process, a difference in thickness (∼50 nm) was occurred between the core layer and the InP side cladding layer. The cross-sectional structure is shown in Fig. [1](#page-2-0) (b) and (c). This ridge structure enhanced the refractive index difference in the lateral direction, which resulted in larger optical confinement than that of the conventional flat structure. After regrowth, the surface was deposited with  $SiO<sub>2</sub>$  as the cladding layer by plasma-enhanced chemical vapor deposition (PECVD) and flattened by chemical mechanical polishing (CMP). After CMP, the thickness of the  $SiO<sub>2</sub>$  layer was approximately 1  $\mu$ m. Subsequently, the wafer was bonded to Si by a-Si-assisted room-temperature surface-activated bonding without annealing. The detailed bonding process is described in [\[19](#page-8-4)[,20\]](#page-8-5). The InP substrate and etch-stop layers were removed by selective wet etching. A 50-nm-deep surface InP grating with a period of 291 nm and duty ratio of 0.5 was defined by electron beam lithography and reactive ion dry etching. Layers of Au/Zn/Au (25/50/300 nm) was deposited by thermal resistance evaporation as *p*-electrode and annealed at 350 °C for 1 min. In addition, Ti/Au (25/200 nm) was deposited as both *p*- and

*n*-electrode. Finally, laser and detector were electrically isolated by removing unnecessary InP, which suppressed the leakage current and crosstalk in the integrated structure. This isolation process was the same with that in our previous work [\[17\]](#page-8-2). After isolation process, about 5-µm width InP layer was remained on both sides of GaInAsP core as cladding layers for a good coupling with LD and PD (Fig. [1\(](#page-2-0)c)).



<span id="page-2-0"></span>**Fig. 1.** Schematic of membrane optical link (a) top view (b) cross-sectional view of active region and absorber (c) cross-sectional view of passive waveguide.



<span id="page-2-1"></span>**Fig. 2.** Fabrication process of membrane optical integrated circuit.

## **3. Static characteristics**

Figure [3](#page-3-0) (a) shows the photocurrent of the p-i-n membrane PD as a function of the laser injection current at various stage temperatures. The reverse bias of PD was −1 V. The wafer surface and stage temperatures were calibrated prior to the measurement. At 25  $^{\circ}$ C, the DFB laser had a low threshold current of 0.27 mA, and the corresponding threshold current density was 386 A/cm<sup>2</sup> due to enhanced lateral optical confinement. The optical saturation current was >8.5 mA and the maximum detected photocurrent was 0.95 mA, which was 6 times larger than that in the previous work [\[17\]](#page-8-2). This increase in the photocurrent is due to the low thermal resistance of membrane DFB laser when introducing the surface activated bonding rather than the conventional BCB bonding. The thermal resistance was measured to be about 510 K/W using another membrane DFB laser which has the same structure with the device shown in Fig. [1.](#page-2-0) This value was  $1/10$ of the previously reported membrane DR laser  $[21]$  with 30-µm length DFB cavity thanks to the BCB-free (surface activated bonding) structure and a little longer DFB cavity length (70  $\mu$ m). The slope of  $I_{LD}$ - $I_{PD}$  was 0.203 mA/mA, which is three times greater than that in the previous work. Although we cannot separately derive a slope efficiency of the integrated SAB membrane DFB laser including coupling and waveguide loss, simple estimated value of slope efficiency using a typical GaInAs PD responsivity of 1 A/W can be 0.203 W/A. At 100 °C stage temperature, a photocurrent of 0.246 mA was still present at a laser injection current of 5.8 mA. The maximum operation stage temperature was recorded at  $120^{\circ}$ C, which was the highest operation stage temperature obtained in this study. Figure [3\(](#page-3-0)b) shows the *I*PD-*V*bias characteristics of the integrated p-i-n PD for various laser bias current at 25 °C. The dark current was 0.29 µA at the bias voltage of −1 V.



<span id="page-3-0"></span>**Fig. 3.** (a) Detected photocurrent as the function of laser injection current at various stage temperature, (b) *I*PD-*V*bias characteristics of the integrated p-i-n PD for various injection currents in DFB laser at 25 °C.

#### **4. Dynamic characteristics**

Figure [4](#page-4-0) shows an image of the SAB-MPIC during the modulation measurement. For electrical connection, 40 GHz and 100-µm-pitch GS/SG-type RF probes were used. The devices were fabricated on a 2-inch wafer, and the measurements were carried out by on-wafer measurements without cleaving. The small-signal frequency response  $S_{21}$  (10 MHz-20 GHz) was measured by a vector network analyzer (VNA). A DC source was supplied to each bias tee, and a DC-coupled signal was applied to the DFB laser via the GS probe. The modulated optical signal was transmitted through the waveguide. The RF component of the p-i-n PD electrical output was separated by a bias tee and entered into the VNA.



<span id="page-4-0"></span>**Fig. 4.** Image of the device during modulation measurement.

Figure [5](#page-5-0) shows the small-signal frequency response and modulation efficiency at various stage temperatures. The p-i-n PD bias voltage was fixed at −3 V. The peak frequency increased with the increase in DFB laser bias current, which indicates that the response is not electrical crosstalk between the two RF probes. The spike near 0.4 GHz was due to the measurement system but not due to the device. The 3-dB bandwidth of the MPIC was 16.8 GHz at a DFB laser bias current of 4.0 mA. The theoretical estimation of 3-dB bandwidth of fabricated membrane PD was about 21 GHz. In addition, 10.3 GHz/mA $^{1/2}$  and 6.8 GHz/mA $^{1/2}$  modulation efficiency were obtained for  $f_{3dB}$  and  $f_r$ , respectively. The modulation efficiency was determined by the slope of the 3-dB bandwidth, and relaxation oscillation frequency was determined as a function of the square root of the bias current above the threshold. These values were comparable to those of our previous study with a similar volume of the active region. When the ambient temperature was higher than the room temperature, 12.1 GHz and 10.1 GHz 3-dB bandwidths were obtained with bias current of 3.2 and 3.0 mA at 50 °C and 80 °C temperature, respectively. The modulation efficiency of 9.3 GHz/mA<sup>1/2</sup> and 6.9 GHz/mA<sup>1/2</sup> were also obtained for  $f_{\rm 3dB}$  at 50 °C and 80 °C, respectively. These values were smaller than those at room temperature since the differential gain decreased with increasing temperature. Figure [6](#page-6-0) shows the small-signal response with different bias voltages of the p-i-n PD for a membrane laser of fixed bias current of 2.0 mA. Increased reverse bias voltage had a larger 3-dB bandwidth due to the strong electric field, which shortened the transit time of the photogenerated carriers. The maximum 3-dB bandwidth was obtained at a bias voltage of −3 V. Additionally, we performed data transmission in the MPIC. The input signal was generated by an arbitrary waveform generator (AWG). A pseudorandom binary sequence (PRBS) of the  $2^{15}$ -1 non-return-to-zero (NRZ) signal was used. The degradation of the signals due to the electrical cables is compensated by the function of the AWG, but no pre-emphasis on the device was applied. The signals from the p-i-n PD were recorded using a sampling oscilloscope. Figure [7](#page-6-1) (a) shows an eye diagram of the 15 Gbps data transmission at various stage temperatures. A clear eye opening of 15 Gbps was obtained at 25, 50, and 80 °C. Figure [7](#page-6-1) (b) shows the maximum data transmission eye diagrams obtained at 25 Gbps and 20 Gbps at 25  $\degree$ C and 50  $\degree$ C, respectively, which are the highest bit rates recorded at room and higher temperatures. These results show that the MPIC has the potential to behave as an optical wiring at various ambient temperatures.



<span id="page-5-0"></span>**Fig. 5.** Small-signal response *S*<sup>21</sup> and modulation efficiency at various stage temperature (a) 25 °C (b) 50 °C and (c) 80 °C.





<span id="page-6-0"></span>**Fig. 6.** Small-signal response of bias voltage dependence with a bias current of 2.0 mA.



<span id="page-6-1"></span>**Fig. 7.** (a) 15 Gbps eye diagram at 25 °C, 50 °C and 80 °C; (b) maximum data transmission eye diagram of 25 Gbps and 20 Gbps at 25 °C and 50 °C, respectively.

#### **5. Conclusion**

In conclusion, we demonstrated an SAB-MPIC with a BRW structure working at various stage temperatures. Large photocurrents of 0.95 mA and 0.246 mA were detected at 25 °C and 100 °C, respectively. The maximum operating temperature was  $120^{\circ}$ C. A high slope of 0.203 mA/mA was obtained at 25 °C. The 3-dB bandwidths of 16.8 GHz and 10.1 GHz were achieved at 25 °C and 80 °C, respectively, and the MPIC was successfully operated at 25 Gbps and 15 Gbps data transmission at 25 °C and 80 °C, respectively. These results show that the SAB-MPIC can operate at various temperatures. To achieve a low power consumption and high-speed SAB-MPIC for on-chip optical wiring in the future, a membrane DR laser will be introduced to increase the efficiency and reduce energy cost. In addition, a low-loss InP waveguide will be introduced to decrease the transmission loss for the cm level data transmission. And a GaInAs bulk p-i-n PD with a short absorber length will be introduced to decrease the junction capacitance and increase the bandwidth of the PD when considering a large load resistor will be used in PD circuit to give a large output drive voltage in the optical wiring application.

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**Data availability.** The data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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